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Influence of Low Thermal Budget Plasma Oxidation and Millisecond Laser Anneal on Gate Stack Reliability in view of 3D Sequential Integration

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Abstract

In this work, we study two approaches to improve gate stack reliability in a low thermal budget process flow in view of 3D sequential integration. For the first time, plasma oxidation at 500°C and millisecond laser anneal are used to obtain a higher interlayer oxide quality, leading to an improvement in reliability. Besides, the benefits of milliseconds laser anneal just after gate aSi deposition is highlighted, which could be linked with the poly-crystallization of the layer upon annealing.

1. Introduction

3D sequential CoolCube™ integration is based on stacked layers of devices fabricated one on top of each other, allowing very small 3D contact pitch (limited only by lithographic performance) and gains in power and performance [1]. One key enabler is then the low thermal budget (TB) processing of top layer devices in order to avoid performance degradation of bottom ones. For hour-scale of processing, the temperature limit is around 500°C, over which bottom silicides start degrading, while higher temperature can be reached when annealing time is concordantly decreased [2]. In that frame, gate stack reliability then becomes one of the main challenges. Indeed, a drastic increase in the flatband voltage shift upon negative bias induced stress is observed when the process flow TB is decreased down to 600°C 1min (Fig. 1). As reported in previous works, this shift is mostly due to creation of dangling bonds and defects in the oxide interlayer (IL) induced by the vertical field [3-4]. In this paper, we study two approaches in order to improve gate stack reliability in a low TB process flow. The first one is based on quality optimization and stabilization of the IL prior to high-k deposition. The second one relies on IL annealing through part of (post high-k) or whole (post amorphous Si deposition) gate stack. For both of these approaches, we present novel low TB processes: Applied Materials decoupled (DPO) or remote plasma oxidation (RPO) at 500°C and Vantage® Astra™ Dynamic Surface Annealing (DSA) milliseconds laser annealing.

2. Experimentals

NMOS capacitors were fabricated on 300mm wafers with process flow given in Fig. 2. Thermal anneal after LPCVD aSi deposition was performed in order to simulate subsequent TB of a MOSFET device: 1050°C spike, corresponding to high temperature junctions activation, and 600°C 1min, corresponding to low temperature SPER (Solid Phase Epitaxy Regrowth) process [5]. In this study, intermediate 525°C 5h anneal was performed on all samples. Decoupled or remote plasma oxidation at 500°C were performed on the chemical oxide in order to obtain a better interfacial layer. In parallel, gate stack annealing was done using DSA milliseconds laser, which allows annealing up to very high temperature over a short time to limit the TB (here, 1100°C, 0.5ms). DSA was done either after HfO_2 or aSi deposition. Reliability was then evaluated by extracting the shift in flatband voltage (ΔV_{FB}) of MOSCAPs induced by different negative bias stresses during 100s at 125°C.

3. Results

Interlayer stabilization

DPO and RPO at 500°C were performed on the chemical oxide in order to obtain a higher quality oxide at low temperature. Consequently, ~1Å increase in EOT is observed with reduced gate leakage following a typical SiO_2/Si barrier trend (Fig. 3). A slight gain in reliability was obtained as compared to untreated chemical oxide reference (Fig. 4a). Nevertheless, this gain is not significant when compared to the 1050°C 2s reference, indicating that IL stabilization is not sufficient for reliability improvement at low TB.

Gate stack annealing

High temperature anneal (T=1100°C) over very short time (t=0.5ms) was then performed either after HfO_2 or aSi deposition by DSA. DSA on HfO_2 led to a slight decrease in EOT of 0.3Å. This gain is due to densification hence reduced thickness of HfO_2, as confirmed by XRR and ellipsometry measurements (Fig. 5). Nevertheless, no significant gain in reliability was obtained, confirming the previous paragraph conclusion (Fig. 4b). On the other hand, DSA after aSi deposition led to a more significant gain (Fig. 4c).

4. Discussions and Conclusions

In this work, the impact of low TB plasma oxidation on chemical oxide was first studied. Higher quality oxide obtained with DPO and RPO at 500°C led to a slight but not significant improvement in reliability, indicating that stabilized IL alone is not sufficient at low TB. In a second time, the effect of milliseconds laser anneal on the gate stack properties was evaluated. While DSA anneal (1100°C, 0.5ms) on HfO_2 yielded almost no improvement in reliability, annealing after aSi led to a more significant decrease in the stress-induced V_{FB} shift. From these results, we expect that poly-crystallization of aSi upon annealing could play a role in improving reliability (Fig. 6). For instance, presence of poly grains could influence the distribution of hydrogen in the stack during forming gas anneal [4]. Polysilicon could also promote the formation of a silicate at the IL/HfO_2 (seen on EDX measurements in Fig. 6) interface which could impact the reliability as well. Nevertheless, further studies will be required to conclude. Within these hypotheses, stabilized oxides (DPO/RPO) combined with ms laser annealing, could be the way to obtain desired reliability at low TB. Furthermore, nanoseconds laser annealing could also be promising for the crystallization of the amorphous layer with a low thermal budget [6-7].

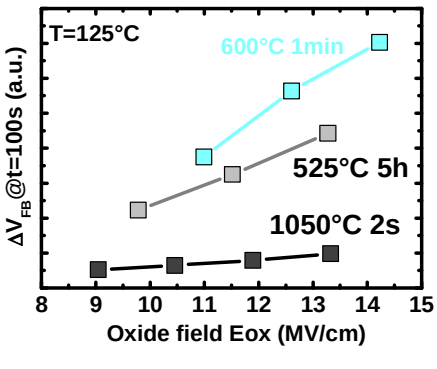

Fig.1: Flatband voltage shift induced by negative gate bias measured on MOS capacitors (50µm*50µm). Low thermal budget leads to a strong degradation of reliability.

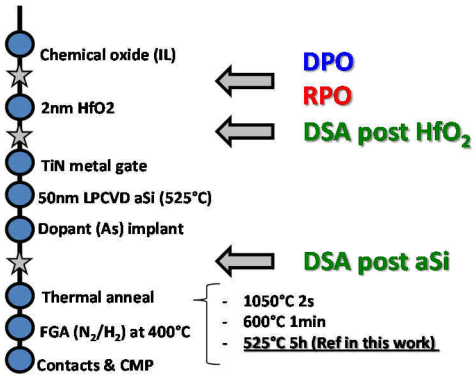

Fig.2: MOS capacitors process flow. 525°C 5h anneal was done on all samples, this TB corresponding to a worst case scenario for subsequent steps (offset spacer deposition, raised source/drain epitaxy…).

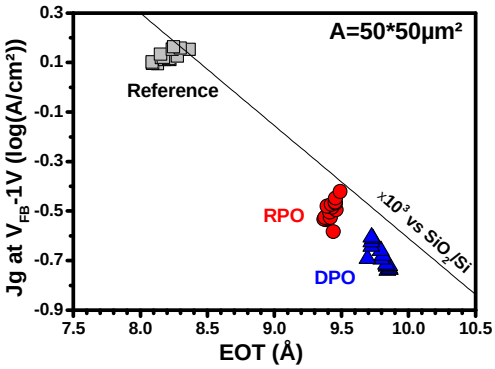

Fig. 3: Gate leakage current versus EOT. Plasma oxidation induced circa 1Å thickening of the chemical oxide.

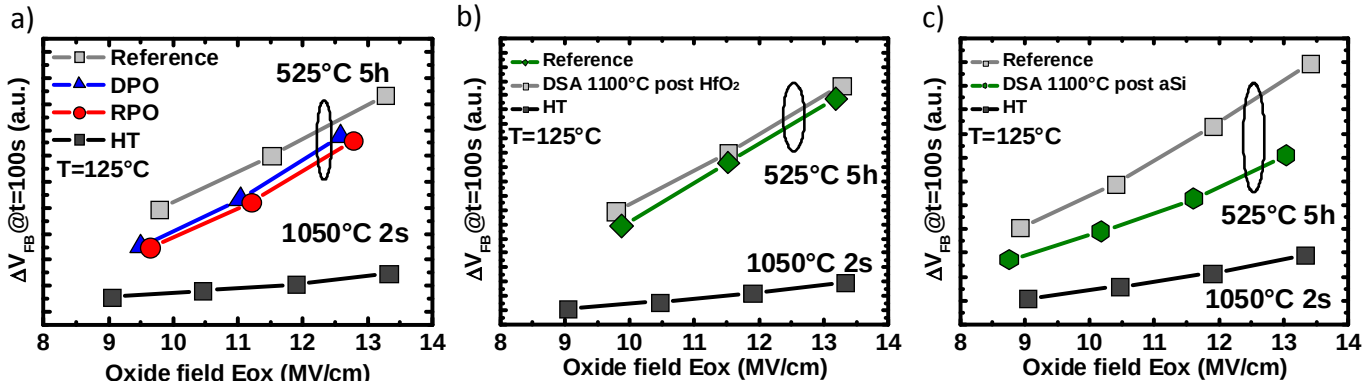

Fig.4: V_{FB} shift induced by negative gate bias. a) Slight improvement of reliability is obtained using plasma oxidation to stabilize the chemical oxide IL; b) almost no improvement is obtained with DSA milliseconds anneal on HfO_2; c) more significant improvement can be obtained with DSA on LPCVD aSi.

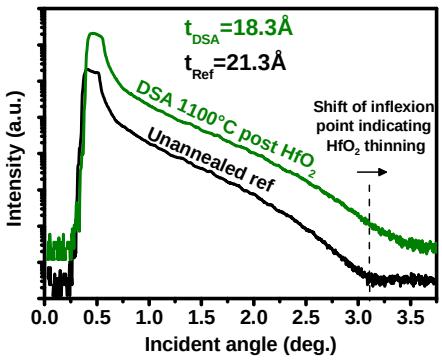

Fig.5: X-Ray Reflectometry measurements showing the densification effect of DSA annealing on HfO_2 and confirmed by the thickness measured by ellipsometry.

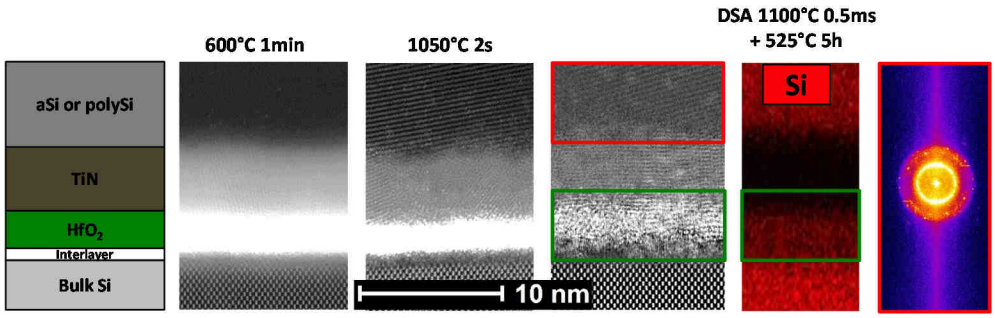

Fig.6: High resolution HAADF (Z-contrast imaging) cross-sectional scanning TEM observations of gate stacks annealed with different thermal budgets. Polycrystalline grains can be observed after a 1050°C 2s or DSA 1100°C 0.5ms anneal. In the latter case, amorphous phases are still present, as indicated by the rings observed in the numerical diffraction pattern of the capping silicon layer area. Besides, EDX measurements show formation of a Hf silicate.

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References: [1] P. Batude et al., Symposium on VLSI Technology (2015); [2] C. Fenouillet-Beranger et al., IEEE Devices Meeting (2014); [3] D. Schroder et al., J. Appli. Phys. 94, 1 (2003); [4] J. Stathis et al., Microelectronics Reliability, Vol 46, Issues 2-4 (2006) [5] L. Pasini et al., International Workshop on Junction Technology (2014) ; [6] I. Ouerghi et al., IEEE MEMS (2016) ; [7] I. Ouerghi et al., IEEE Devices Meeting (2015).