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Enhanced Electrical and Reliability Characteristics in Ge p-MOSFETs by In-situ Plasma Treatments and Capping Hf/Zr on Interfacial Layers

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Abstract

A Ge p-MOSFET with an ultralow equivalent oxide thickness (EOT) of ~0.47 nm and a high hole mobility of ~401 cm^2/V-s is demonstrated in this work. The excellent electrical characteristics are obtained by in-situ H_2 and NH_3 plasma treatments on the Ge/high-k interface. The enhanced drive current can be attributed to the lower EOT or higher mobility. Device with a Hf cap layer demonstrates the lowest interface trap density and stress-induced leakage current. Moreover, device with Zr cap layer has the lowest hysteresis effects and stress-induced voltage shifts.

1. Introduction

Germanium has been widely studied as the most promising candidate of channel material because both electron and hole mobility are about two and four times higher than those of silicon. However, the most critical thing is the formation of excellent interfacial layer (IL) between the high-k dielectric and Ge substrate. Many papers about the treatments for ILs have been reported, such as O_2 plasma [1], H_2O plasma [2], and desorption [3] processes. Although the equivalent oxide thickness (EOT) can be scaled down, the interface properties need improvement. It is reported that hydrogen incorporation is effective to reduce interface traps of Ge MOS devices due to the H^+ passivation at GeO_2/Ge interface [4], and electrical characteristics are improved by ZrO_2/HfO_2 stack gate dielectric [5]. Therefore, in-situ H_2 and NH_3 plasma treatments and Hf/Zr capping layers on ILs are investigated in this work.

2. Experimental

After dilute HF clean (HF:H_2O=1:100) for 10 mins to remove the native oxide, a remote H_2O plasma is in-situ applied to form GeO_2 IL in an atomic layer deposition (ALD) chamber at 250 ^oC and a power of 300 W. Then, plasma treatments with H_2, NH_3 and NH_3+H_2 are performed, respectively. Afterwards, Hf or Zr-rich cap is in-situ deposited in ALD at 250^{o}C on some samples. Then, a 3-nm thick HfO_2 or ZrO_2 is in-situ deposited as gate dielectrics. Next, a 100-nm thick TiN film is deposited by sputtering as metal gate, and a post metal annealing is performed at 550 ^{o}C for 30 s. A BF^{2+} ion implantation with an energy of 25 keV and a dose of 5x10^{15}cm^{-2} is performed. A 300-nm thick Al film is deposited as contact electrodes of source and drain. Lastly, a forming gas annealing is carried out at 400^{o}C for 10 mins.

3. Results AND Discussion

Fig.1 illustrates device structure and process flows. Fig. 2 shows I_D-V_G for Ge MOSFETs with H_2, NH_3 and NH_3+H_2 plasma treatments on ILs. The I_{OFF} can be lower for sample with NH_3 plasma treatment. Fig. 3 shows I_D-V_D for all samples. The I_{ON} of sample with H_2 plasma treatment is the highest. Fig. 4 shows that I_g versus V_g curves for all samples are similar. Fig. 5 shows C-V characteristics for all samples, indicating an EOT value of ~0.47 nm. Fig. 6 shows (a) S.S. and transconductance, and (b) mobility of all samples. Sample with H_2+NH_3 plasma treatment has the lowest S.S. values and highest mobility. Fig. 7 shows peak hole mobility versus EOT of samples in this wrok with some published data in literatures. Sample with NH_3+H_2 plasma treatment can obtain a lower EOT and a high mobility.

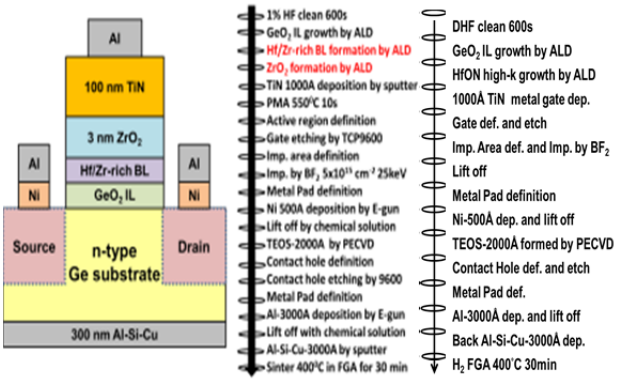

Fig. 1 Devices structure and process flows of Ge MOSFETs.

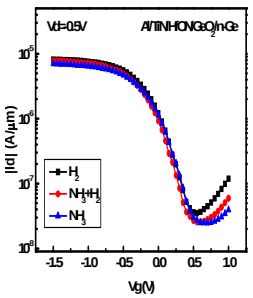

Fig. 2 I_D-V_G of samples with in-situ plasma.

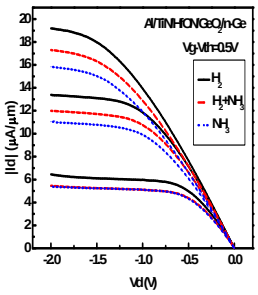

Fig. 3 I_D-V_D of samples with in-situ plasma.

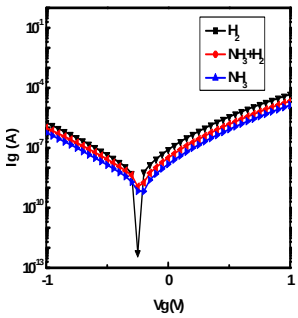

Fig. 4 I_G-V_G of samples with in-situ plasma.

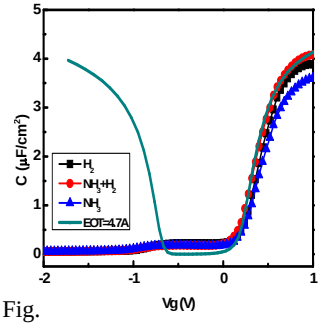

Fig. Fig.5 C-V and EOT extraction of sample with in-situ plasma.

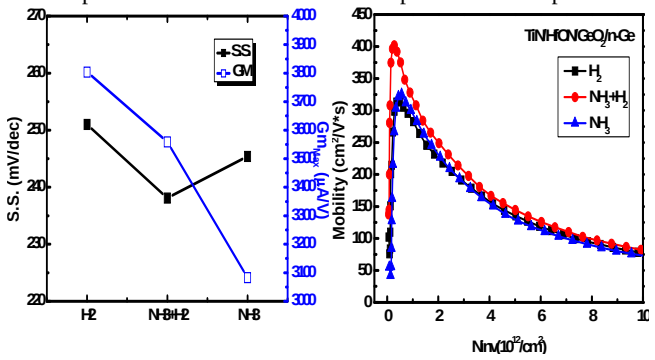

Fig. 6 (a) S.S & G_m and (b) hole mobility of samples with in-situ plasma.

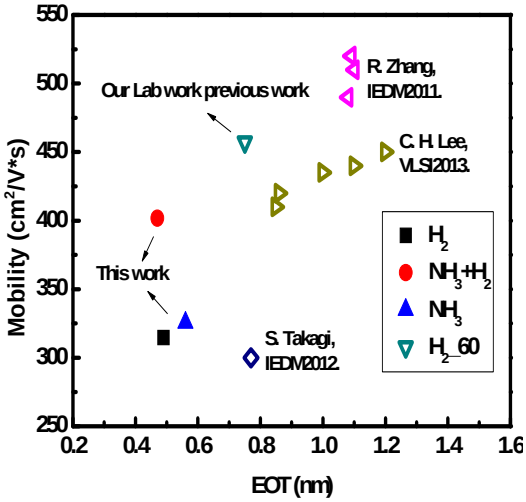

Fig. 7 Peak hole mobility versus EOT of all samples with some benchmarks.

Fig. 8 shows that C-V curves and EOT values are slightly changed by capping Hf/Zr on IL. Fig. 9 shows cross-sectional TEM pictures of samples w/o or with Hf/Zr capping. Fig. 10 shows hysteresis values for samples w/o or with Hf/Zr capping, suggesting hysteresis effects can be reduced by capping a Hf or Zr on ILs. Fig. 11 shows interface trap density (D_{it}) of all samples. Sample with Hf capping demonstrates the lowest D_{it} value because more GeO_x with oxidation state of +4 can be obtained in $HfGeO_x$. Fig. 12 shows stress-induced (a) flat-band voltage shift and (b) leakage current (SILC). Sample with Zr capping has the lowest flat-band voltage shift, and sample with Hf capping demonstrates the lowest SILC value.

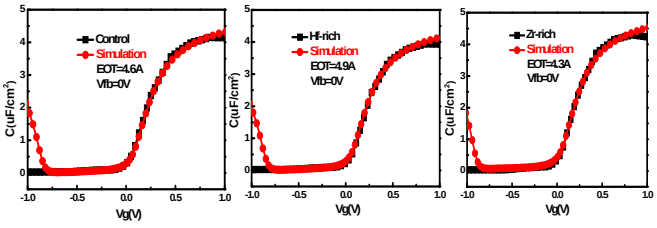

Fig. 8 C-V data and EOT of samples w/o or with capping.

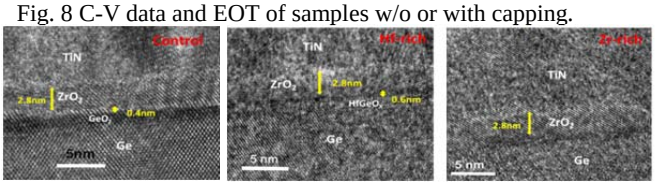

Fig. 9 Cross-sectional TEM of (a) w/o, (b) Hf, and (c)Zr capping on IL.

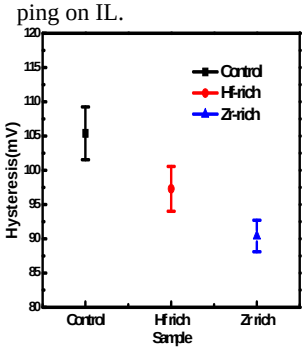

Fig. 10 Hysteresis values of samples w/o or with capping.

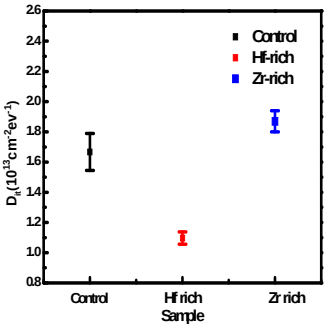

Fig. 11 Dit for samples w/o or with capping.

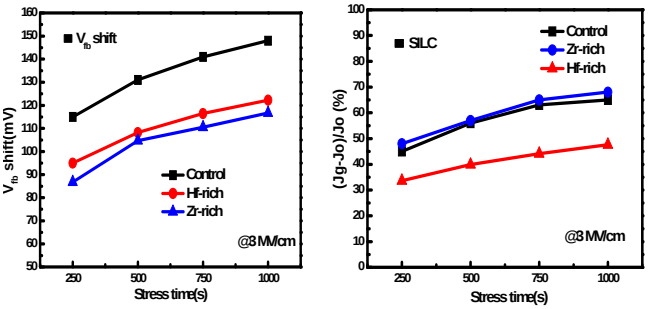

Fig. 12 Stress-induced (a) flat-band voltage shifts, and (b) leakage current of samples w/o or with capping.

4. Conclusions

An EOT of ~0.47 nm and a peak hole mobility of ~401 cm^2/V-s in Ge p-MOSFETs are obtained by a NH_3+H_2 plasma treatment. The interface traps can be minimized by a Hf cap layer, and the oxide traps can be reduced by a Zr cap layer. Therefore, electrical and reliability characteristics in Ge MOS devices can be improved by in-situ plasma treatments and Hf or Zr capping on ILs..

References

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