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A Self-Terminated Energy-Efficient Nonvolatile Flip-Flop Using 3-terminal Magnetic Tunnel Junction Device

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Abstract

A nonvolatile flip-flop (NV-FF) is proposed for a zero-standby-power LSI using a 3-terminal magnetic tunnel junction (3T-MTJ) device. The use of self-terminated mechanism, which continuously monitors the change in MTJ resistance, makes it possible not only to minimize energy consumption during backup operation but also to assure reliable write. Moreover, since the write current path is separated from the read current path in the 3T-MTJ device, the sensing circuit and the write driver are individually optimized, which makes it possible to reduce performance overhead due to additional components. As a result, the backup energy of the proposed NV-FF is reduced by 64% compared to that of a conventional NV-FF using worst-case-oriented writing scheme with small performance overhead.

1. Introduction

A nonvolatile flip-flop (NV-FF) is an essential component for the nonvolatile logic LSI since temporal data of each function block must be clock-synchronized and backed up before power-off [1, 2]. A magnetic tunnel junction (MTJ) device is one viable candidate to implement the NV-FF owing to its virtually unlimited endurance, CMOS compatibility, and 3-dimensional stacking capability [3-5]. However, the stochastic nature in MTJ switching is an important issue in the MTJ-based NV-FF design. Because worst-case-oriented long-time write current pulse is required for reliable MTJ switching, the backup energy is high. To overcome this issue, a self-terminated NV-FF, which makes it possible to minimize backup energy by monitoring the voltage change in MTJ switching and terminating write current, has been proposed [6]. Meanwhile, a performance overhead due to the additional function potentially exists and minimization of the overhead is an important design consideration. A 3-tetminal MTJ (3T-MTJ) device is focused on to realize nonvolatile logic LSI [7-9]. Since the write current path is separated from the read current path in the 3T-MTJ device, the sensing circuit and write driver are individually optimized, which is quite attractive for logic circuit design. In this paper, a self-terminated mechanism is applied to the 3T-MTJ based NV-FF [9] and its effectiveness is discussed.

2. Self-Terminated NV-FF Using 3T-MTJ device

Figure 1 (a) shows a symbol of the 3T-MTJ device. A binary data is written as resistance value (R_0 or R_1) by applying a bi-directional write current I_{WR} between T2 and T3. The data is read by applying a read current I_{RD} between T1 and T3. The *R-I* characteristic of the 3T-MTJ device is shown in Fig. 1 (b). Figure 2 shows the schematic diagram of the proposed NV-FF, which is composed of a nonvolatile master latch and a CMOS-based slave latch. The nonvolatile latch is implemented by using a CMOS-based latch, a 3T-MTJ-based nonvolatile storage cell, and a self-termination circuit. During basic operation, these components are disabled and separated by the CMOS pass gates so that they do not affect the circuit performance. Figure 3 shows the schematic diagram of the self-termination circuit. At the beginning of backup operation, STR becomes low and WE is pre-charged. Then, STR becomes high and voltage monitoring is started. If the desired data is written (Y=A), the output signal of the completion detector (DONE) becomes high. Then WE is discharged and backup operation is terminated. Figure 4 shows a schematic diagram of the 3T-MTJ-based storage cell. The resistance of the 3T-MTJ device is read by the voltage division between the PMOS transistor and the NMOS transistors with the 3T-MTJ device [8]. The bi-directional write current is driven by two CMOS inverters when WCK and WE are become high. Owing to its 3T structure, the transistor size of the inverters is optimized without considering the sense margin; the sense margin can be independently optimized by the sizing of the PMOS transistor and the NMOS transistor in the sensing circuit.

3. Evaluations

For the evaluation, the proposed NV-FF is designed using 90-nm CMOS technology together with an MTJ device model [10] whose parameters are shown in Table I. Figure 4 shows the basic behavior of the proposed NV-FF. We can confirm that temporal data are stored into the 3T-MTJ device and the write current is automatically terminated immediately after the desired data is written. We can also confirm that if Nq = M, backup operation is skipped. Table II summarizes a comparison of MTJ-based NV-FFs. Since the write driver and sensing circuit are individually optimized, the active power consumption and the propagation delay are small compared to the previous works. Note that, the active power consumption of the Ref. [9] is relatively high because CMOS inverters in the master latch are used for the write driver and their size must be enlarged. To demonstrate the impact of the proposed self-terminated mechanism, the backup energy of the 8-bit NV-FF is evaluated. In this evaluation, the typical switching time of the 3T-MTJ device and its standard deviation are set 5ns and 10%, respectively. In accordance with these parameters, the worst-case switching time is estimated about 10 ns. As a result, the backup energy is reduced by 64% compared to that of worst-case-oriented

write scheme as shown in Table III.

4. Conclusions

An energy-efficient self-terminated NV-FF using 3T-MTJ device has been presented. It is expected that the use of the 3T-MTJ device can explore wide variety of applications owning to its logic-circuit-design friendly structure.

Acknowledgements

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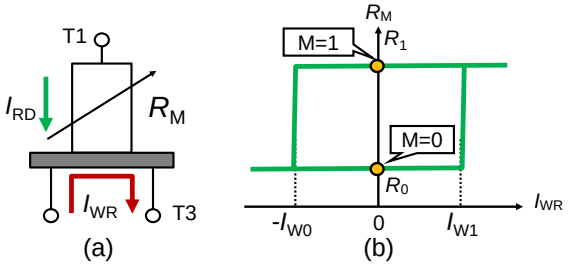

Figure 1. 3T-MTJ device: (a) structure, (b) R-I characteristic.

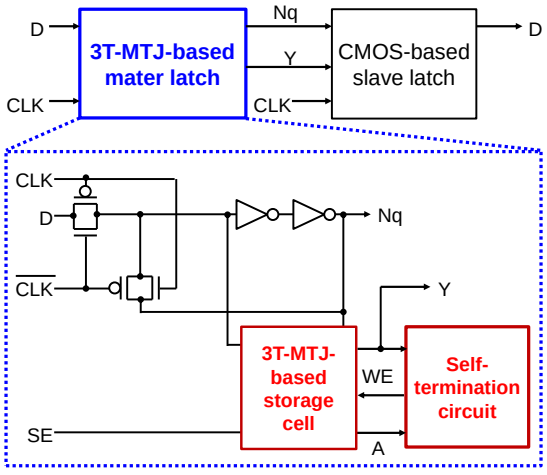

Figure 2. Schematic of the proposed NV-FF.

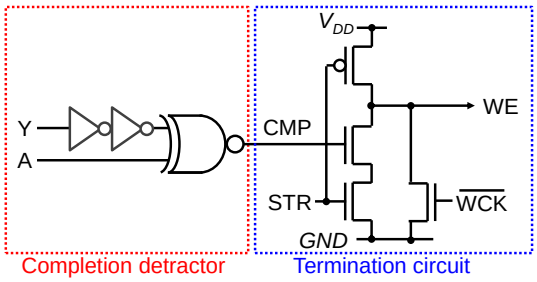

Figure 3. Schematic of the self-termination circuit.

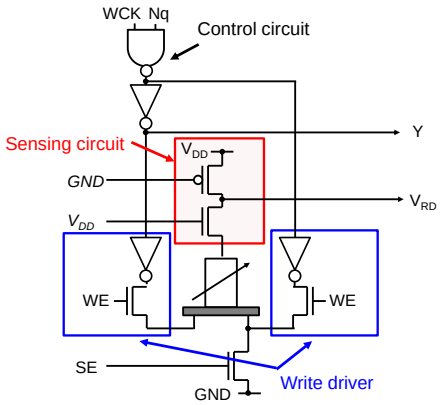

Figure 4. Schematic of the 3T-MTJ-based storage cell.

TABLE I. Design parameters

R_0	R_1	I_{W0}	I_{W1}
8 kΩ	24 kΩ	-0.08 mA	0.08 mA

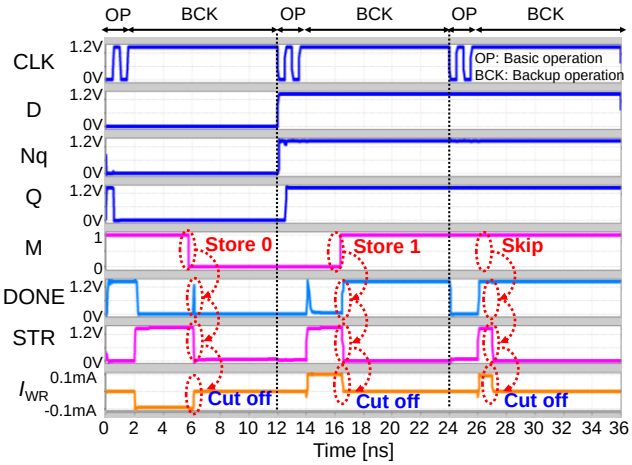

Figure 5. Basic behavior.

TABLE II. Performance comparisons.

	Ref. [9]	Ref. [6]	**Proposed**
Device	3T-MTJ	2T-MTJ	**3T-MTJ**
Self-termination	No	Yes	**Yes**
Transistor counts*1)	23	46	**47**
Active power [μW] *1, 2, 3)	10.0	8.54	**8.05**
Delay [ps] *1, 2, 4)	67.9	64.1	**59.7**
PDP [μW*ps] *5)	679	522	**480**

*1) Input buffer, output buffer, and clock buffer are not included.
*2) 90nm CMOS technology (V_{DD} = 1.2V).
*3) Average power during normal operation at 1.0 GHz.
*4) Maximum time from V_{CLK} crossing 50% to V_Q crossing 50%.
*5) PDP: Power-delay product.

TABLE III. Average backup energy of 8-bit NV-FF.

	Worst-case-oriented (Conventional)*3)	**Self-terminated (Proposed)**
Average backup energy [pJ] *1, 2)	9.6 pJ	**-64% 3.5 pJ**

*1) The number of iteration is 100.
*2) Random patterns are applied to the input.
*3) The width of the write current pulse is fixed to 10ns.