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Spin Hall Effect-based Asynchronous Nanomagnetic Logic Devices

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Abstract

Effective implementation of nanomagnetic logic (NML) in system level architectures has been seriously constrained by inefficient interconnects and poor error tolerant designs. These issues arise due to limitations in precise clocking and utilization of field coupled interconnects. In this work, we propose spin Hall effect (SHE) based asynchronous NML devices with charge based interconnects as a potential alternative for traditional in plane-NML devices. The majority gate design, used as a building block to realize several other NML devices/architectures is demonstrated here.

1. Introduction

The application of nanomagnetic logic devices [1] in realistic system/chip level architectures has been constrained due to critical issues such as, poor error tolerance and in-efficient interconnects. Reliable switching of NML devices/architectures mainly depends on clocking process, i.e., simultaneously setting a group of nanomagnets to align along their hard axes. However, this process is highly sensitive to fabrication reliability, geometric misalignments and thermal noise, which are almost impossible to be avoided at room temperature [2]. Particularly, in case of multiphase clocking, clocking zones have to be stringent to ensure successful alignment of magnets. Even 1% deviation in field alignment could result in incorrect logic operation of 75% of gates; therefore, precise control over clocking is required.

To overcome this issue, in this work, we propose SHE-based asynchronous NML devices without the need for clocking. Pure spin currents generated by SHE are used to switch input magnets and majority of fields acting on output magnet decides its magnetization state. Due to SHE, charge currents flowing through heavy metal with strong spin orbit coupling generate pure spin currents with polarization perpendicular to both charge and spin current directions [3]. In traditional NML devices, clocking is mainly used to reduce the energy barrier of output magnet and control the data flow i.e. from input to output, not vice versa, while, in this novel design, input magnets are engineered to be thicker and harder than the output magnet so that enough magnetic field is generated to switch the output magnet without reducing its energy barrier and to ensure that output does not affect inputs. In addition, field coupled interconnects in NML architectures consume huge energy and area, and result in long delays, particularly in case of global interconnects. Hence, we realized charge based interconnects using dual MTJ model [4] for our design**.** The proposed majority gate can be used as AND/OR/NOR gates by fixing one or more inputs and can also be used as building block for several NML architectures like full adders, multipliers, FFT layouts, etc.

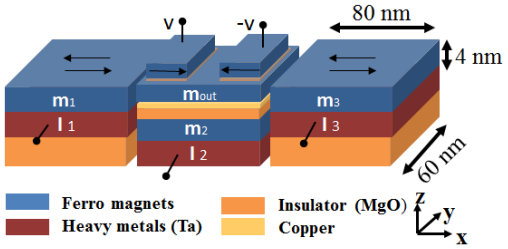

Fig.1. Spin Hall Effect-based three-input NML majority gate.

2. Simulation Methodology

As shown in Fig. 1, SHE-based three-input majority gate is studied using Object Oriented Micro Magnetic Framework (OOMMF) software [5]. The three input nanomagnets m_1, m_2, and m_3 are magnetically coupled to the output magnet m_{out}. Nanomagnets m_1, m_3, and m_{out} are ferromagnetically coupled (FM), while m_2 and m_{out} are antiferromagnetically coupled (AFM). Input nanomagnets are switched using pure spin currents and the majority of fields generated by m_1, m_2, and m_3 would determine the final magnetization state of m_{out}. For our simulation, input magnets with volume of 80 nm×60 nm×4 nm, saturation magnetization of 800 emu/cm^3 and coercivity of 230 Oe are considered. The critical spin current density required for magnetization reversal of input nanomagnets is estimated as $5.106 \times 10^{10}\ A/m^2$. This critical spin current can be generated by passing 28 μA charge current through tantalum of dimensions of 60 nm, 80 nm, 2 nm, spin Hall angle of 0.3 and resistivity of 200 μΩ−cm^2. As mentioned above, output nanomagnet is considered to be thinner and softer than input magnets i.e. with volume of 80 nm×60 nm×2 nm and coercivity of 110 Oe. To switch the output magnet, the resultant magnetic field acting on m_{out} due to m_1, m_2, and m_3 should be greater than its coercivity i.e. 110 Oe. To obtain this magnetic field, m_1, m_{out}, and m_3 are placed at a distance of 8 nm between each other and m_2, m_{out} with distance of 15 nm between them. The magnetic field induced by m_1 or m_3 on m_{out} is given by $\vec{H}_{FM}$ and field created by m_2 on m_{out} is given by $\vec{H}_{AFM}$. The tensor components of $\vec{H}_{FM}$ and $\vec{H}_{AFM}$, H_{FM} and H_{AFM} are shown in Eq. (1) and (2), respectively. Finally, to read m_{out} electrically, two MTJ with oppositely magnetized pinned layers are connected to positive and negative voltages ($\pm v$), respectively. Depending on magnetization state of m_{out}, a bipolar current output ($\pm I_{out}$) can be achieved. Using resistance area product of 18 μΩ−cm^2 and v of ±0.32 V, I_{out} of ± 40 μA can be obtained.

$$H_{FM} = \begin{bmatrix} Hxx & Hxy & Hxz \\ Hxy & Hyy & Hzy \\ Hxz & Hyz & Hzz \end{bmatrix} = \begin{bmatrix} 116 & 0 & 0 \\ 0 & -37 & 0 \\ 0 & 0 & -78 \end{bmatrix} \quad (1)$$

$$H_{AFM} = \begin{bmatrix} Hxx & Hxy & Hxz \\ Hxy & Hyy & Hzy \\ Hxz & Hyz & Hzz \end{bmatrix} = \begin{bmatrix} -120 & 0 & 0 \\ 0 & -172 & 0 \\ 0 & 0 & 292 \end{bmatrix} \quad (2)$$

3. Results & Discussion

Operating Principle

Due to FM coupling between m_1, m_3 and m_{out}, magnets m_1 and m_3 try to align m_{out} towards their own magnetization states while due to AFM coupling between m_2, and m_{out}, nanomagnet m_2 tries to align m_{out} opposite to its magnetization state. The truth table of majority logic gate is given in Table I, followed by Fig.2 (a-h) illustrating the operation of the majority gate with input current directions for all cases shown in Table I, respectively. It can be understood from Table I and Fig.2, that by fixing m_2 to 0, two-input OR gate can be realized and by fixing m_2 to 1, two-input AND gate can be realized.

Switching Mechanism

Switching mechanism of majority gate considering four different cases using spin current density of $2 \times 10^{11}\ A/m^2$ is shown in Fig. 3(a-d). Magnetization dynamics of precessional switching, where m_1 and m_3 are fixed to opposite magnetization states and m_2 is switched from -1 to 1, which switched m_{out} from 1 to -1 due to AFM coupling is shown in Fig.3 (a). While m_2 is in dynamic state, large perpendicular field is acted on m_{out} as shown in tensor H_{AFM} in Eq. (2), resulting in precessional switching. Next, the magnetization dynamics of damping switching is shown in Fig.3, where m_1 and m_2 are fixed to same magnetization states and m_3 is switched from 1 to -1, which in turn switched m_{out} from 1 to -1 due to FM coupling. However, due to weak perpendicular field acting on m_{out} when m_3 is in dynamic state, switching is

TABLE I
TRUTH TABLE OF MAJORITY GATE

Inputs			Output
m_1	m_2	m_3	m_{out}
0	0	0	0
0	0	1	1
1	0	0	1
1	0	1	1
0	1	0	0
0	1	1	0
1	1	0	0
1	1	1	1

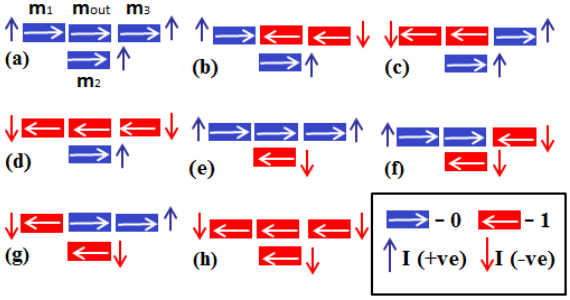

Fig.2. Operation of SHE based majority gate with all switching cases (a-h) as mentioned in Table I, respectively.

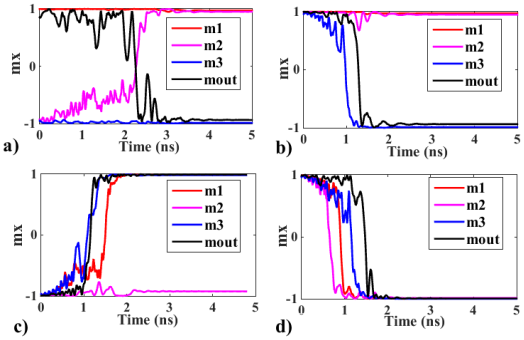

Fig.3. Switching dynamics of m_1, m_2, m_3 and m_{out} w.r.t time a) precessional switching b) antidamping-like switching c) when only m_1 and m_3 are changed d) when all three inputs are changed.

solely due to longitudinal field as shown in tensor H_{FM} in Eq. (1) resulting in antidamping-like switching. Similarly, Fig.3 (c) shows the magnetization dynamics of m_1, m_2, m_3 and m_{out}, when only m_1 and m_3 are switched from -1 to 1. Finally, magnetization dynamics of m_1, m_2, m_3 and m_{out} is shown in Fig.3 (d), where all three inputs are changed from 1 to -1. The switching time of input and output nanomagnets in all four cases is different from each other due to stray fields acting on each of them due to the other.

Performance Evaluation

For performance evaluation, we compared SHE-based NML 1-bit full adder with traditional NML full adder using SHE based pipelined clocking, assuming the same simulation parameters for both designs. It was observed that the proposed SHE-based design is 40 times better than traditional design in terms of energy delay area product. This marked improvement in performance characteristics is due to elimination of number of driving and interconnects magnets. Moreover, external circuits used to clock traditional NML devices can also be eliminated by proposed design. However, scaling of this novel design is limited as two MTJ's with considerable size have to be placed on output magnet and input magnets have to be stronger than output magnet.

4. Conclusion

In this paper, spin Hall effect based asynchronous NML device is proposed. Realization of asynchronous NML device using charge based interconnect has resulted in less complex, easy to fabricate, more realistic NML architectures with significantly improved performance characteristics, for instance 40 times improvement in energy delay area product in case of 1-bit full adder.

Acknowledgements

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