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Improvement of Silicon Nanowire Solar Cells Made by Metal Catalyzed Electroless Etching and Nano-imprint Lithography

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Abstract

Silicon nanowires were fabricated by metal catalyzed electroless etching (MCEE) and Nano-imprint lithography (NIL), then core-shell p-type layer was grown by thermal chemical vapor deposition (CVD) techniques. In order to reduce back surface recombination effect and also to activate dopant, we used two techniques to improve device performance by back surface field and rapid thermal annealing. In this study, we optimized the conditions and improved the device performance and the efficiency achieves from 4.1% to 7.4% (MCEE device) and from 1.1% to 6.6% (NIL device) after BSF and RTA treatment. Moreover, to reduce the reflectance after the shell formation, selective area etching method was investigated.

1. Introduction

As a clean and renewable energy, solar energy has been burgeoning advanced in the past several decades which the bulk silicon (Si) solar mastered the major market due to its high efficiency. However, the high cost of silicon wafer reduces its cost-competitive. In recent years, with enormous advantages of carrier collection, light absorption and particularly low cost of Si, Si nanowire (SiNW) solar cells offer a potential to replace the bulk Si solar cells.

Despite such advantages of SiNW solar cells, the industrialization is still in the early stage. Especially relatively lower efficiency compared with bulk silicon solar cells becomes a problem. To improve the performance, some methods had been investigated. A technique called "back surface field" (BSF) was proved as a useful method for bulk Si solar cells which consists of a higher doped region of the rear surface of the solar cell. The interface between the high and low doped regions introduces a barrier to minority carrier flow to the rear surface which reduce back surface recombination. Furthermore, the purpose of rapid thermal annealing (RTA) is to activate dopant atoms to obtain the desired electronic contribution from dopants in a semiconductor, which is widely used in bulk solar cells production.

In a previous work [1], to get a good metal contact with the front surface, all of nanowires were embedded in the p-Si matrix. However, the reflection was increased due to the embedded sturucture. To solve this problem, a selective etching method is being investigated [2], which is protecting the metal electrode area by photolithography. By using the etching process, the protected area was not etched while nanowire structure was formed in the unprotected area.

In this paper, we report the effect of the back surface field and rapid thermal annealing of two kinds of Si solar cells by Metal-Catalyzed Electroless Etching and Nano-imprint lithography. Thermal CVD was used for the formation of boron (B) doped p-type shell layer. Photo J–V curve showed that solar cell efficiency was improved by BSF and RTA treatments. Following the experiments, selectively etching was done to improve the reflection after the shell growth by CVD.

2. Experimental

SiNW arrays were prepared by Metal-Catalyzed Electroless Etching (MCEE) and Nano-imprint lithography (NIL) on 525 μm-thick n-type crystalline Si (111) substrates. Then, all samples were put into CVD chamber to fabricate solar cell junction by deposition of the B-doped p-type Si shell layer. Finally, a finger grid Al pattern and full coverage Ag were sputtered for front and back electrode contacts. The main process is shown in Fig. 1. SEM images of nanowire arrays by MCEE and after CVD shell growth are shown in Fig. 2.

Rapid thermal annealing was performed after forming the shell layers at 950 °C for 3 min in an N_2 environment by ULVAC QHC furnace. The back surface field was created by spin coating of phosphorus-containing solution (OCDP-59210) and simultaneously prebaked at 450 °C for 30 min and annealed at 850 °C for 45 min in N_2 flow.

For the selectively etching process, first, photoresist layer was spun on the surface of silicon substrate, then Photolithography technique was used to develop the selective area for etching.

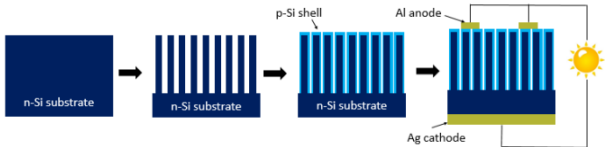

Fig. 1. Schematic diagram of preparing Silicon Nanowires Solar Cell.

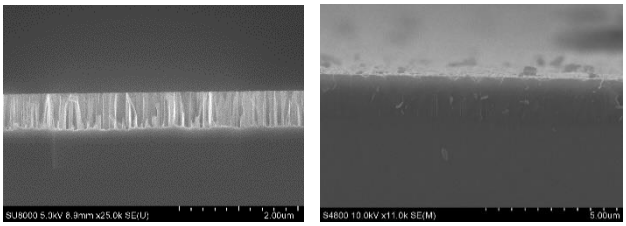

Fig. 2 (a) Silicon nanowire arrays were prepared by MCEE. (b) After CVD shell growth, NW arrays were embedded in a p-Si matrix.

3. Results and discussion

Fig. 3(a) and Table I shows the current-voltage (JV) curves under 100 mW/cm^2 illumination of MCEE processed Si nanowire solar cells. For the BSF treated samples fill factor (FF) was increased from 0.39 to 0.62, while V_{OC} and J_{SC} remain, as compared to reference sample, resulting in the efficiency improvement from 4.1% to 6.6%. These results clearly indicate the the BSF formation reduces the back surface recombination. By combining BSF and RTA-treatment the Jsc and Voc further increase to 24.18 mA/cm^2 and 0.50V, finally the efficiency increases to 7.4%. The improvement is due to the dopant activation effect.

Fig. 3(b) and Table II, shows the NIL processed silicon nanowire solar cells. For the BSF treated sample in NIL process also have an clear improvement in the performance of solar cells. The Jsc, Voc and FF increases from 10.62 to 25.38 mA/cm^2, 0.36 to 0.48V, 0.28 to 0.37, respectively. Eventually, efficiency increases from 1.1% to 4.5%. Furthermore, by combining BSF and RTA-treatment FF was improved greatly to 0.54 which enhance the efficiency to 6.6%. As a result, BSF and RTA process improved the device performance of both MCEE and NIL processed samples.

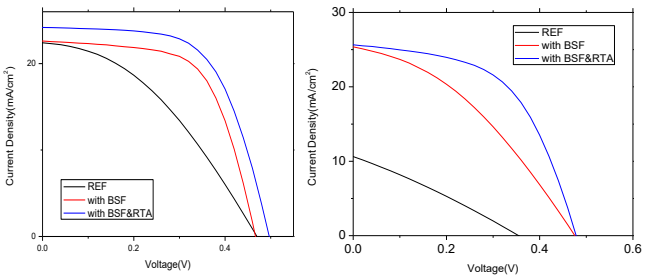

Fig.3 (a) I-V curves of MCEE samples. (b) I-V curves of NIL samples.

Table I Parameters of MCEE samples

	J_{SC} (mA/cm^2)	V_{OC} (V)	FF	Eff. (%)
REF	22.42	0.47	0.39	4.1
With BSF	22.62	0.47	0.62	6.6
With BSF&RTA	24.18	0.50	0.61	7.4

Table II. Parameters of NIL samples

	J_{SC} (mA/cm^2)	V_{OC} (V)	FF	Eff. (%)
REF	10.62	0.36	0.28	1.1
With BSF	25.38	0.48	0.37	4.5
With BSF&RTA	25.65	0.48	0.54	6.6

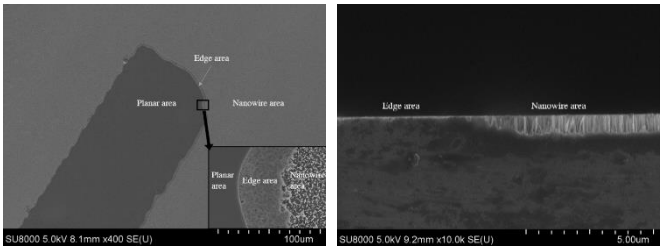

Fig. 5 (a) Top view of selective etching silicon substrate. (b) Cross-section view of selective etching silicon substrate.

Fig 5(a) shows that a top-view SEM image of selective area etching done by a photolithography technique. Nanowire area was selectively etched by MCEE process. Fig 5(b) shows that cross-sectional SEM image of selectively etched Si nanowire area and the edge of protected area. The selectively etching qualitatively improves the metal contact for Si nanowire solar cells. The optimized condition of device and the device performance are still under research.

4. Conclusions

We reported here that process of fabricating Si nanowire solar cell by two different methods. To obtain better performance of the device, BSF and RTA method was applied and optimized. Due to the desirable effect of reducing back surface recombination and dopant activation the efficiency of Si nanowire solar cells was improved to 7.4% of MCEE and 6.6% of NIL. The device performance clearly indicates that BSF and RTA are significantly enhanced the device performance either base on MCEE or NIL. Moreover, in order to reduce reflection after CVD shell growth, selectively etching method was investigated, SEM results were discussed and the effect of device performance are still under research.

Acknowledgements

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