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Design and Characterization of Logic Compatible Drain Extended FinFETs for Embedded High-Voltage Circuits

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Abstract—As a general trend, when technology scales, the maximum sustainable voltage decreases accordingly. The maximum operation voltage is typically limited by high surface electric field at the drain junctions in off-states transistors. This work presents a drain extended FinFET (DE-FinFET) structure employing a lightly-doped drain and a floating field plate in 16nm CMOS technologies. Lightly-doped drain increases the breakdown voltage of p-n junction while floating field plate alleviates the corner electric field at drain junction edge. Measurement data reveals that this DE-FinFET design can easily raise the gated breakdown voltage without process modifications.

1. Introduction

As the technologies advances to nano-scale dimensions, the maximum operational voltage a transistor can sustained generally decreases with its maximum supply voltages [1]. In 3D FinFET technologies, the maximum drain voltage allows is reduced to less than 3V. However, in multi-functional embedded ICs, it generally requires a wide range of operational voltages for modules other than logic circuits [2-4]. It is hence imperative to provide special high-voltage (HV) devices by either structure modifications and/or process adjustment for the circuits operates under voltages large that supplied voltages [5-6]. Extended drain structure and field plates are commonly adopted design for high-voltage MOSFETs in 2D planar transistors [7-10]. In this work, these two structure modifications are applied to 3D FinFETs, followed by comprehensive characterization of new HV devices.

2. Device Structure

As discussed above, the transistor's breakdown voltage is known to reduce significantly as technology node scaled to nano-meter range. The gated breakdown characteristics (at V_G=0) of transistors from different technology nodes are compared in Figure 1. As indicates in the I_D-V_D characteristics, the breakdown voltage are reduced to less than 3V in 16 nm FinFETs. The cross-sectional illustration of the proposed DE-FinFET structure is illustrated in Figure 2(a), where the floating metal gate (FMG) acts like as the field plate and extended drain regions is defined by a lighter doped n-well, as depicted in the device layout in Figure 2(b). In a FinFET, see the 3D structure illustrated in Figure 2(c), the n^+ regions are formed by SiP epitaxial growth. The highly abrupt pn junction will lead to small breakdown voltages. In the DE-FinFET, SiP n^+ is enclosed by the n-well to ensure intrinsic junction breakdown will not limit the overall maximum voltage. As the field plate length larger, the on-state current is smaller. The floating field plate consists of a short metal gate is placed above the lighted doped drain region The FMG coupled by the drain voltage alleviating the band-bending at the drain junctions. By reducing the high surface electric field, the breakdown voltage can be enhanced thereafter. The simulated I_D-V_D curves is compared to that from real measurement results, as shown in Figure 3. Good agreement between the measured and simulated data suggest that a well-established 3D structure is achieved.

3. Device Optimization

The measured threshold voltages and on-state current of the DE-FinFETs with different field plate length (L_{FP}) are summarized in Figure 4. It is found that as L_{FP} increases, the threshold voltage of the overall transistor increase slighted, while the on-state current degraded significantly. The specific on-resistance (R_{on}) of this devices is compared to off-state current in DE-FinFET of increasing L_{FP} in Figure 5. It is found that the off-state current is independent of the field plate length, as the leakage current is dominated potential distribution at the drain junction edge. The breakdown characteristics on samples prepared by 16nm FinFET technologies are measured and compared in Figure 6. When gate is floating, the junction's intrinsic characteristics can be measured. Data in Figure 6 shows that the breakdown of DE-FinFET can be effectively extended. Figure 7 summarize the gated breakdown voltage and off-state current vs. DE-FinFET with increasing L_{FP}. As expected, L_{FP} have very little effect on transistor leakage as well as breakdown voltages. The breakdown voltage and $R_{on\text{-}sp}$ with different field plate length shown in Figure 8, suggesting that further scaling of L_{FP} effectively reduces $R_{on\text{-}sp}$, while not affecting its breakdown voltages.

4. Leakage Current Analysis

Off-state leakage current is discussed in the following section. First, the temperature effect on off-current (at V_D = 3.3V, V_G=0V) and breakdown voltage shown in Figure 9 reveals that the off-state current increases significantly with raising temperature. To further understand the sources of leakage in the DE-FinFETs, the off-state current characteristics at different field plate gate voltages (V_{FP}) are compared in Figure 10. Data reveals that negative V_{FP}, promoting band-to-band (BTB) tunneling at the drain junction, can significantly affect the low field leakage current. Figure 11 and Figure 12 further analyze the activation energy of the off-state leakage current at different V_{FP}. With enhance BTB tunneling effect at negative V_{FP}, Table 1 summarized the basic characteristics of the optimized DE-FinFETs, demonstrating a good logic compatible HV devices.

5. Conclusions

In this paper, we present a drain extended FinFET realized by 16nm high-k metal gate CMOS technology for 5V-operation. Experimental data suggest that Drain Extension (DE) FinFET combining the new floating field plate and lightly-doped extended drain can be applied in high-voltage circuits in nano-CMOS FinFET technologies.

Acknowledgement

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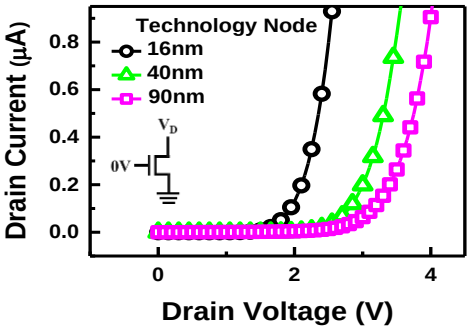

Figure 1 As the technology scales, the gated-breakdown voltage reduces aggressively.

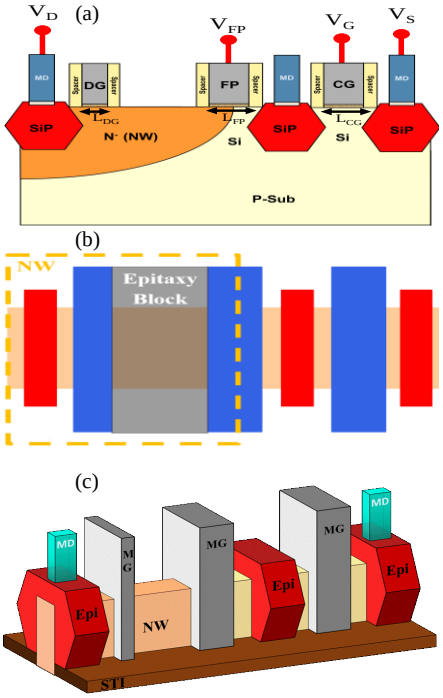

Figure 2 (a) Cross-sectional view of DEMOS. (b)Layout of the DEMOS. (c) 3D illustration of the DEFinFET with extended drain region.

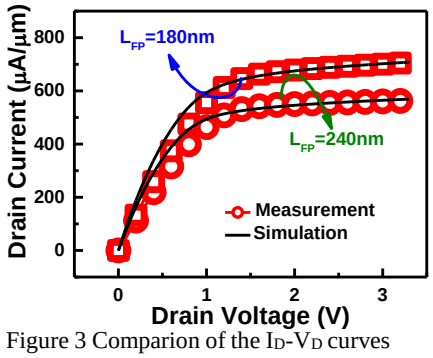

Figure 3 Comparion of the I_D-V_D curves by simulation and measurement data.

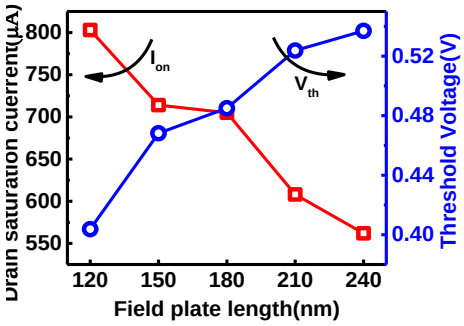

Figure 4 Threshold voltage and on-current (@V_{FP}=V_G=1.8V) for DEFinFETs with different field plate length.

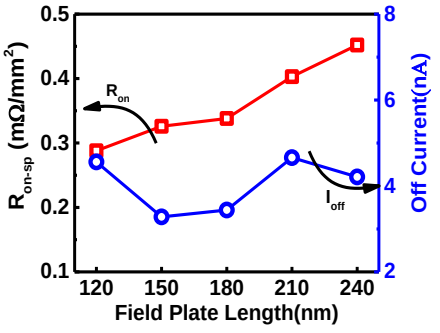

Figure 5 Specific on-resistance and off–state current of DEFinFETs with different field plate length ranging from 120~240 nm.

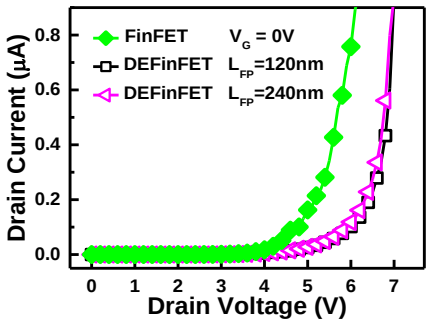

Figure 6 Measured gated breakdown characteristics of the DEFinFETs comapares with standard FinFET devices..

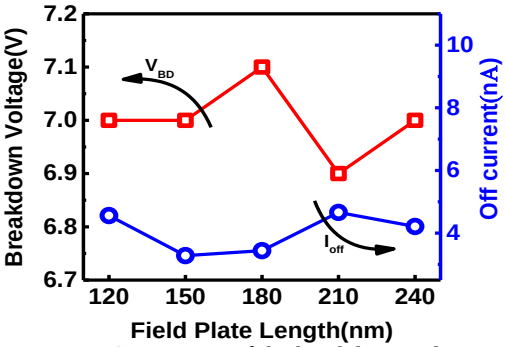

Figure 7 Comparison of the breakdown voltage and off-state leakeage current of DEFinFETs vs field plate length by simulation results.

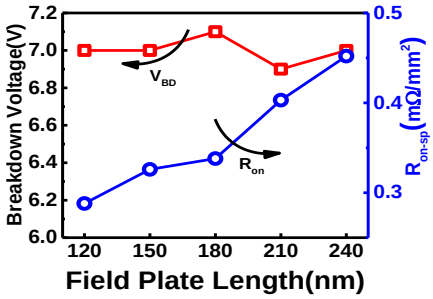

Figure 8 Specific on-resistance of DEFinFET and breakdown voltage vs field plate length, shows minimal Ron at short L_{FP}.

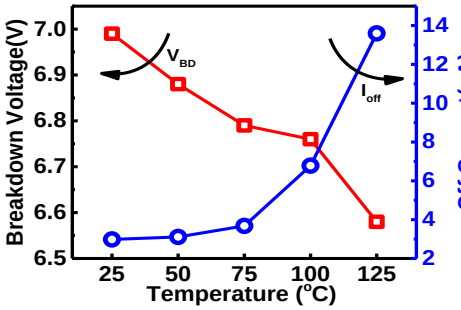

Figure 9 Temperature effect on off current (@V_D=3.3,V_G=0V) and the breakdown voltagse of DEFinFETs with differnet L_{FP}.

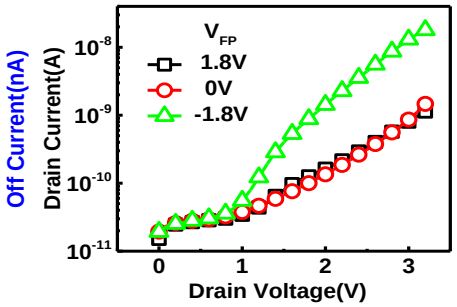

Figure10 Leakage characteristis of DEFinFETs at different field plate voltage indicating the drain leakage current are dominated by BBT current.

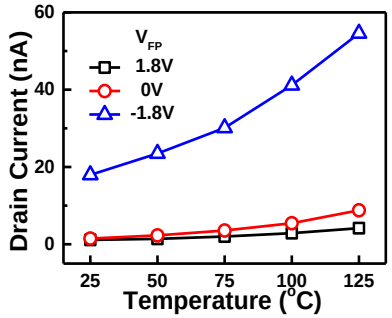

Figure 11 Temperature effect on off-current at different V_{FP}. Negative V_{FP} induced BTB tunnelting promotes I_{off}.

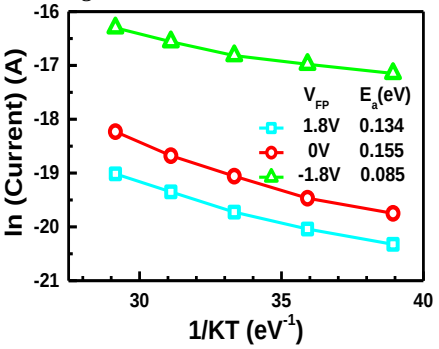

Figure 12 Activation Energy of off-state current of DEFinFETs at different V_{FP}.

	Simulated	Measured
L_{FP}(nm)	120	120
I_{on}(uA/um)	802	803
I_{off}(nA/um)	27.2	4.56
V_{BD}(V)	6.7	7
R_{on-sp}(mΩ/mm²)	0.246	0.288

Table 1 Summary table of the performance parameters of DEFinFET for 5V operation, comparing measured and simulation results.