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Impact of the 3D Stacking Power Supply on Chip for High Frequency DC-DC Converter

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Abstract

In this paper, a buck converter using Gallium Nitride High Electron Mobility Transistors (GaN-HEMT) was simulated with LTspice. This simulation shows the efficiency at high frequency more than 10MHz. We evaluated the 3D power SoC at 3mm square chip and revealed 87% efficiency is provided in the circuit. Moreover, this paper will evaluate the impact of parasitic on converter performance.

1. Introduction

The power supply on chip (power SoC) which integrates passive components such as inductors and capacitors with semiconductor devices attracting attentions because it can realize ultimate miniaturization of the power supply [1]. The switching frequency of the power SoC are required more than 10MHz. Increasing the efficiency is one of the important issues for power SoC and to minimize parasitic capacitance and inductance are effective ways to do this. The GaN power device is attractive because it has inherent advantages of high frequency switching and high voltage capability. The conventional PCB based assembly technology cannot extract the performance of GaN power devices [2].

In this paper, we propose the 3D power SoC (Fig.1), which stacks GaN power device, Si-LSI and passive devices. In addition, we describe the impact of the 3D stacking structure for high frequency power supply based on electro-magnetic and circuit simulations.

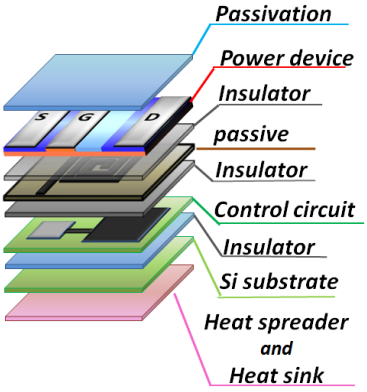

Fig. 1 The image of 3D power SoC

2. Electromagnetic and circuits simulations

We use LTspice for circuit simulations. The circuit diagram is shown in Fig. 2. The buck converter is used. Input voltage is 5 V and output voltage is 2.5 V. In this study, we use EPC8007 (GaN power device) as a switching and rectifier devices [3]. The chip size was optimized for each switching frequency under constant Ron・Qg. This means that LTspice parameter was changed for each switching frequency. We assumed the size of power SoC is 3 mm X 3 mm. The inductor is simulated using HFSS (High Frequency Electromagnetic Field Simulation [4]) and these results are used in circuit simulations. The simulated structure is shown in Fig. 3. The results are listed in Table 1. The trench capacitor was analyzed using analytical model as follows. The simulated structure is shown in Fig. 4. The capacitance and the ESR in this simulation are 0.494[μF] and 76.5[μΩ] when the trench diameter and depth are 1.0 μm and 20.0 μm, respectively. The capacitance was calculated by eq. (1).

$$C = \varepsilon_0 \varepsilon_{SiO_2} \cdot S_{SiO_2} / d_{SiO_2} \qquad (1)$$

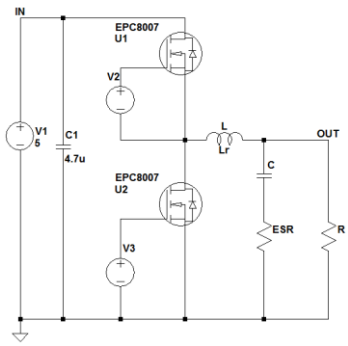

Fig. 2 simulation circuit

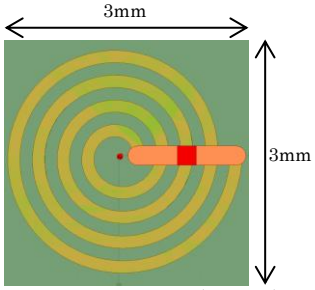

Fig. 3 Inductor (4turn)

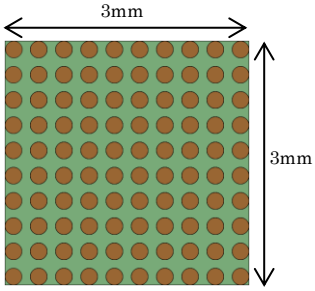

Fig. 4 Trench capacitor

Table 1 Value of inductors for each frequency

3turn	Frequency [MHz]	30	40	50	60	70	80	90
	L [nH]	9.235	9.184	9.148	9.117	9.093	9.072	9.056
	Lr [Ω]	0.0706	0.0853	0.0994	0.1122	0.1236	0.134	0.1437
4turn	Frequency [MHz]	10	20	30	40	50	60	70
	L [nH]	19.025	18.985	18.971	18.916	18.856	18.807	18.767
	Lr [Ω]	0.109	0.121	0.124	0.1492	0.1739	0.1966	0.2172

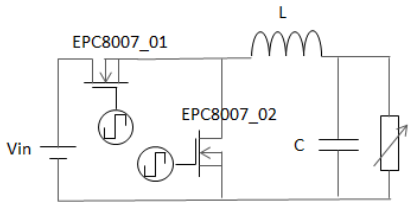

Fig. 4 Buck converter (Vin=5V)

3. Result and discussion

Dependence of the output current on the efficiency is shown in Fig. 5. The maximum efficiency is 87.5% at 0.4A and 40MHz. The efficiency increases with increasing switching frequency at smaller load current. On the contrary, it increases with decreasing frequency at larger current.

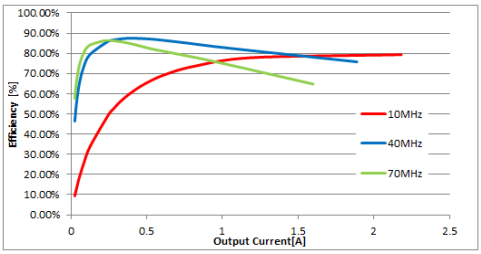

Fig. 5 Efficiency vs Output Current (Vin=5V)

Dependence of efficiency on frequency is shown in Fig. 6. The efficiency slightly increases with decreasing output power. The optimum frequency which gives the highest efficiency increases with decreasing output power. Efficiency is 86.1% when the output power is 2W at 30MHz.

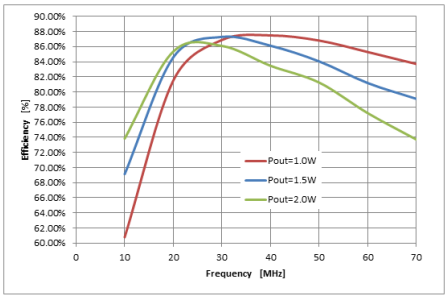

Fig. 6 Efficiency vs Frequency

Figure 7 shows comparisons of the efficiency of the proposed 3D stacked power SoC with state-of-the-art GaN based DC-DC converter [5]. The switching frequency is 40MHz. The efficiency of the-state-of-the-art DC-DC converter is simulated using parasitic value which listed Table 2 and equivalent circuit model shown in Fig. 8 [5]. For the 3D stacked power SoC, thickness of interlayer insulator is assumed 1 μm. Efficiency of the 3D stacked power SoC is always higher than state-of-the-art GaN based DC-DC converter.

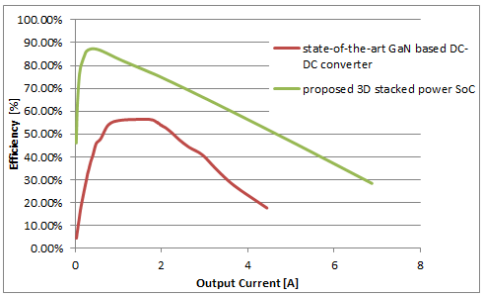

Fig. 7 Comparison of efficiency at 40[MHz]

Table 2 Parasitic model [5]

	L[nH]	R[mH]
Lpg_1	5.74	2.63
Lpd_1	0.66	0.37
Lps_1	0.12	0.15
Lpg_2	7.53	3.02
Lpd_2	0.20	0.24
Lps_2	0.49	0.20

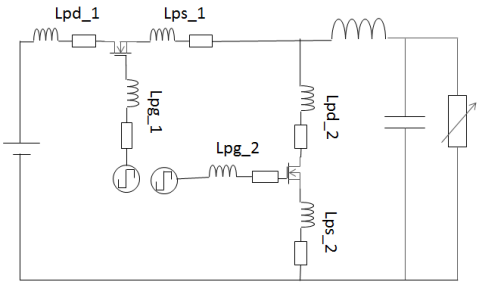

Fig. 8 the-state-of-the-art DC-DC converter parasitic model

4. Conclusions

We clarify the potential of 3D stacked power supply on chip and its impact for high frequency DC-DC converter. The results show that the efficiency of the proposed 3D power SoC is 87.5% at output power 1W, 40MHz, and 3mm square. The efficiency of the 3D stacked power SoC is always higher than state of the art GaN based DC-DC converter.

References

[1] power SoC

[2] G.H.Aghdam, IEEE APEC pp.413-414 2015

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[4] HFSS

[5] D.C.Reusch, Virginia Polytechnic Institute and State University Doctor thesis, p.192, 2012.