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AC Hot carrier effect of the thin-film SOI Power n-MOSFET

Daiki Takenaka and Satoshi Matsumoto

Kyushu Institute of Technology,
Sensui-cho, Tobata-ku, Kitakyushu-shi, Fukuoka, 804-8550, JAPAN
Phone/Fax:+81-93-884-3234, e-mail:p349517d@mail.kyutech.jp

Abstract

This paper describes the hot carrier effect of the thin-film SOI power n-MOSFET under DC and AC stress. In addition, dynamic operation also enhances the device degradation caused by hot carrier effect. In this paper, we reveal Drain Avalanche Hot Carrier (DAHC) effect caused by AC stress strongly affect the device degradation of on-resistance (R_{on}).

1. Introduction

Power ICs fabricate using SOI technology have become attractive because they can completely isolate the devices each other. The thin-film approach has been quite promising because it can reduce parasitic capacitance and induced thermally leakage current.

In power ICs, power MOSFETs usually are used of dynamic operation, but detailed analysis for hot carrier effect under AC stress have not been reported.

This paper reports how DAHC under AC stress. And we reveal DAHC is promoted the device degradation of R_{on} by increasing rise time (t_r) and fall time (t_f).

2. Device structure and Fabrication process

The schematic cross section of the fabricated thin-film SOI power n-MOSFET is shown in Fig. 1 [1]. The body contacts were formed to suppress the parasitic bipolar effect. The main structural parameters are listed in Table. 1. The thin-film SOI power MOSFET was fabricated using the 1.2-μm-rule polyside gate process with local oxidation of silicon (LOCOS) isolation. The main device characteristics of n-channel are listed in Table. 2.

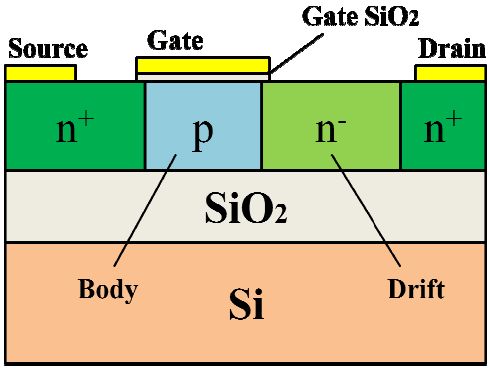

Fig.1 Schematic cross section of SOI power n-MOSFET

Table.1 The main structural parameter

Static characteristics (SOI power n-MOSFET)	
Threshold voltage (mV)	525
On-Resistance (Ω)*	750
Breakdown voltage(V)**	14.4

*V_g=5(V) **V_g=0(V)

Table.2 Device characteristics

Top Si layer(μm)	0.14
Buried oxide(μm)	0.4
Gate oxide(nm)	1.2
Channel Length(μm)	0.5
Drift Length(μm)	0.5

3. Result & Discussion

3-1.DC stress

Dependence of the degradation of R_{on} and V_{th} shift on the stress gate voltage is shown in Fig. 2. The ΔR_{on} degradation has a peak when the stress gate voltage is (Vth+0.2) V. It decreases gradually with increasing the stress gate voltage [3].

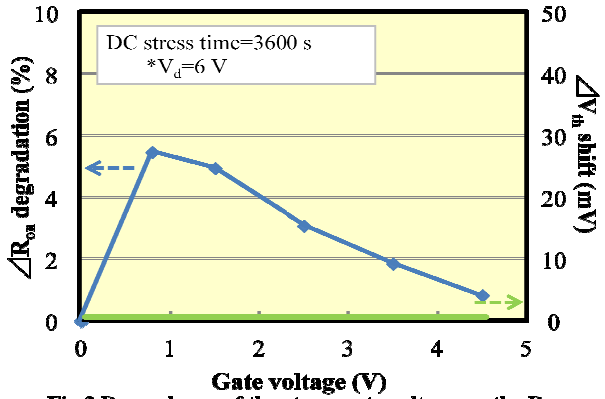

Fig.2 Dependence of the stress gate voltage on the R_{on} degradation rate and V_{th} shift [DC stress]

This trend shows that DAHC strongly depends on the electric field distribution under gate oxide of the thin-film SOI n-MOSFET (Fig.3). The high electric field concentrates near the gate edge of the drain junction when the stress gate voltage is near threshold voltage. This concentration promotes parasitic bipolar effect. On the other hand, we cannot observe V_{th} shift and this mean that Channel Hot Carrier (CHC) effect does not occur.

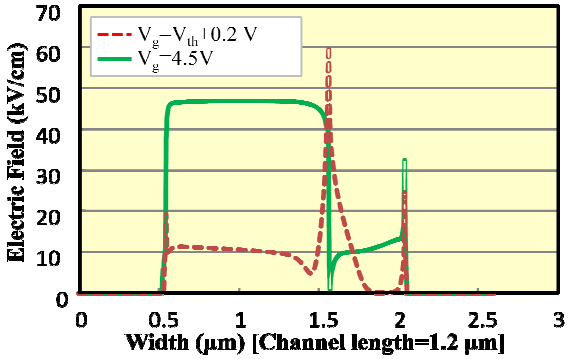

Fig.3 The electric field distribution of a thin film SOI power n-MOSFET

3-2.AC stress

Dependence of R_{on} on the switching frequency is shown in Fig. 4. Dependence of V_{th} shift on the switching frequency is shown in Fig. 5. R_{on} degradation and V_{th} shift under AC stress are larger and higher than those under DC stress because 1 cycle of AC stress has two modes as shown in Fig.6.

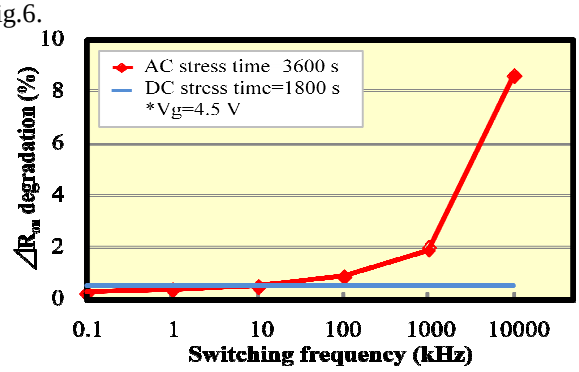

Fig.4 Dependence of the switching frequency on the R_{on} degradation rate [DC and AC stress]

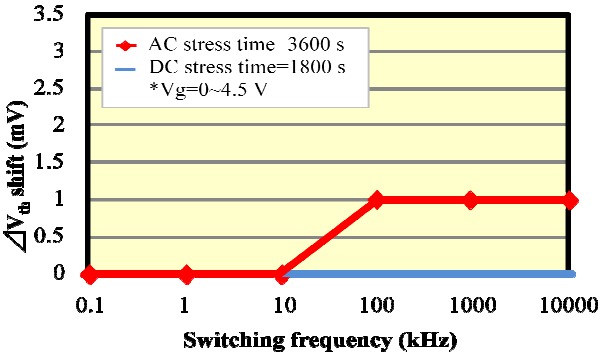

Fig5. Dependence of the stress gate voltage on the V_{th} degradation rate [DC and AC stress]

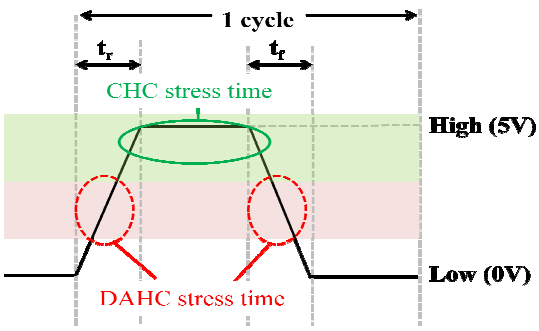

Fig.6 Pulse wave form applied to gate electrode [Duty ratio=50 (%), t_r and t_f=5 (ns)]

R_{on} degradations under AC stress increase exponentially from 10 kHz with increasing the switching frequency. We must take account of two switching parameter: duty ratio, t_r and t_f to reveal which parameter strongly depends on the device degradation. Dependence of R_{on} on the duty ratio is shown in Fig. 7. It has no dependent on duty ratio despite of long CHC time. Dependence of R_{on} on t_r and t_f is shown in Fig. 8. It increases with increasing t_r and t_f.

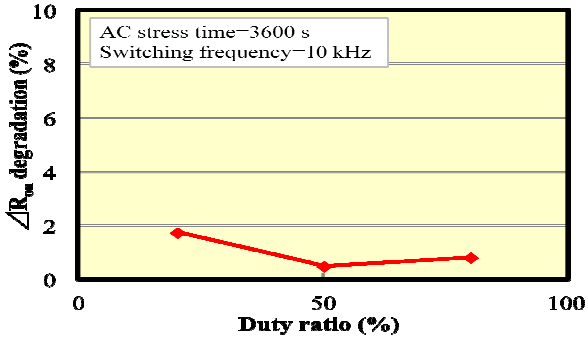

Fig.7 Dependence of duty ratio on the R_{on} degradation rate [AC stress]

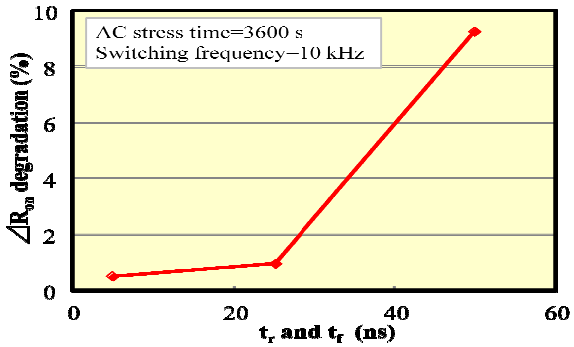

Fig.8 Dependence of t_r and t_f on the R_{on} degradation rate [AC stress]

These results show the device degradation caused by AC hot carrier effect depends stronger on DAHC stress.

4. Conclusions

We investigated DC and AC hot carrier effect of the thin-film SOI power n-MOSFETT. Device degradation caused by AC hot carrier stress is larger than that of DC one. DAHC effect enhances R_{on} degradation. DAHC effect caused by parasitic bipolar effect depends on the switching frequency and dV/dt.

References

[1] J. P. Colinge: Silicon-on-Insulator Technology: Materials to VLSI (Kluwer Academic, Dordrecht, 2004) 3rd ed..
[2] S. Matsumoto, I. –J. Kim, T. Fukumitsu, T. Sakai, and T.Yachi, IEEE Trans. Electron Devices, 43 1998 105.
[3] T. Takasugi and S. Matsumoto, Jpn. J. Applied Physics, vol.53, No.4, 04EP17,2014.