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A Surface-Potential-Based Reverse-Transfer Capacitance Model for Vertical SiC DMOSFET

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***Abstract*—We propose a surface-potential-based reverse transfer capacitance model of SiC power MOSFET for accurate circuit simulations. By considering the physical structure of vertical power SiC MOSFETs, the proposed model can reproduce the reverse transfer capacitance upon wide range of bias voltages. Through experiments using a commercial SiC MOSFET, it is demonstrated that the proposed model can achieve twice more accurate in simulating the reverse transfer capacitance characteristic than the conventional one.**

1. Introduction

Excellent electrical properties of Silicon Carbide (SiC) [1] have improved the efficiency of power converters that operate at high switching frequencies. As the operating frequency of the power converters becomes even higher, circuit simulations become increasingly important. To accurately estimate high-frequency switching behaviors, capacitance model of SiC power MOSFET is important. Among others, modeling of gate-drain capacitance C_{gd}, which is also called as reverse transfer capacitance C_{rss}, is particularly important [2].

As shown in Fig. 1(a), C_{gd} in a vertical double-diffused MOSFET (VDMOSFET) can be considered as a series connection of two capacitors: the oxide capacitance C_{oxd}, and the depletion-layer capacitance of the MOS structure C_{dep}. In the conventional models [3,4], C_{gd} is approximated by connecting two equations that represent the above two capacitors, which are non-differentiable at the gate-drain flat-band voltage V_{fbd} which is the connection point. Besides, the conventional C_{dep} model is expressed as a PN junction capacitor, which ignores the effect of carriers provided when the hole channel is formed. These issues lead to inaccurate circuit simulations.

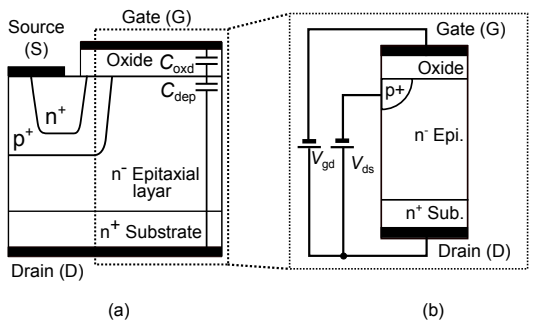

Fig. 1. Cross section of the VDMOSFET.

In this paper, we propose a surface-potential-based C_{gd} model. The proposed model can accurately reproduce bias voltage dependencies by considering the physical behaviors of SiC VDMOSFETs.

2. Surface-Potential-Based C_{gd} Model

C_{gd} consists of C_{oxd} and C_{dep}. The depletion-layer capacitor is formed at the surface of the n-type MOS interface. The thickness of the depletion layer depends on both gate-drain voltage V_{gd} and the potential of the p^+ region, i.e., V_{ds} as shown in Fig. 1(b). The drain-source voltage V_{ds} dependency of C_{gd} is called *body effect*, which should be modeled to realize accurate simulation. In the proposed model, the three-terminal capacitance model [5,6] is adopted. C_{dep} now becomes a function of the surface potential ϕ_{gd} of the channel formed on the drain region under the gate oxide with consideration on the body effect.

From the charge neutrality condition at the MOS interface, the following equation holds:

$$-Q_{gd} = \varepsilon_{SiC} E_{SiC} = \varepsilon_{ox} E_{ox}, \tag{1}$$

where Q_{gd} is the charge density at the MOS interface, ε_{ox} and ε_{SiC} are the permittivities of gate oxide and SiC, respectively. E_{SiC} and E_{ox} are the magnitude of electric fields in SiC substrate and in the gate oxide. Here, $\varepsilon_{SiC}E_{SiC}$ and $\varepsilon_{ox}E_{ox}$ are represented as Eqs. (2) in the next page and (4), respectively:

$$\varepsilon_{ox} E_{ox} = C_{ox} V_{ox} = C_{ox}(V_{gd} - V_{fbd} - \phi_{gd}), \tag{4}$$

where V_{ox} is the voltage across the gate oxide. In Eq. (2), ϕ_t, C_{ox}, N_D, and q are the thermal voltage, the gate-oxide capacitance per unit area, the donor concentration, and the elementary charge, respectively.

A nonlinear equation for the surface potential is derived by substituting Eqs. (2) and (4) for Eq. (1). By numerically solving the equation, the surface potential ϕ_{gd} is derived.

The derivative of the charge density Q_{gd} with respect to ϕ_{gd} gives the depletion-layer capacitance C_s of the three-terminal MOS structure between gate and drain terminals as shown in Eq. (3) in the next page. The V_{ds} dependence in the above equation expresses the body effect. Because C_s is the unit-area capacitance, C_{dep} is calculated by $C_{dep} = A_{gd} \cdot C_s$, where A_{gd} is the area of gate-drain overlap.

Finally, C_{gd} is computed as a series connection of the two capacitors, $C_{gd} = C_{oxd} \parallel C_{dep}$, which is always valid for all bias voltages.

3. Experimental Results

The proposed C_{gd} model, as well as the conventional model [3], is implemented using Verilog-A language. The simulations are conducted by a commercial circuit simulator (SIMetrix Technologies, SIMetrix).

C_{gd} is fitted to the measurement result of a commercial SiC power MOSFET (ROHM, SCT2450KE). Figure 2 shows the fitting results of the conventional and the proposed models to the measured C_{gd} at 1 MHz. As can be seen in the figure, the proposed model achieved better accuracy than the conventional one. Root mean squared errors of the simulated values by the proposed and conventional models are 1.47 pF and 2.80 pF, respectively. Besides, by considering the body effect, V_{gd} dependence of the capacitance better fits to the measured capacitance when $-V_{gd}$ is slightly positive in Fig. 2. Figure 3 shows the derivatives of C_{gd}. The derivative of the conventional model diverges to negative infinity when V_{gd} approaches to V_{fbd}, which is 0.1 V in this example. On the other hand, the proposed model shows smooth transition about that voltage through the computation of the V_{gd} dependence of the surface potential. In our experiments, the proposed simulation model is twice more accurate than the conventional one.

The evaluation of the transient analysis is conducted using a double pulse tester [7]. The drain current I_d, the drain-source capacitance C_{ds}, and the gate-source capacitance C_{gs} characteristics, are also modeled based on the surface potential equation that is similar to the proposed model. In the double pulse tester, the supply voltage is 100 V, the gate resistor is 47 Ω, and the load inductance is 380 μH. Diode-connected SCT2450KE is used as a free-wheeling diode. The parasitic elements of the packages and the passive components have been included in the simulation. Figure 4 shows the simulated and the measured waveforms of I_d, gate-source voltage V_{gs}, and V_{ds}. From the figure, the proposed model can accurately simulate the transient characteristics.

4. Conclusion

In this paper, we proposed a surface-potential-based C_{gd} model for accurate circuit simulation using SiC power MOSFETs. The proposed C_{gd} model is based on the physical construction of the SiC power VDMOSFET. The experimental results show that the proposed model can reproduce C_{gd} more accurately than the conventional one.

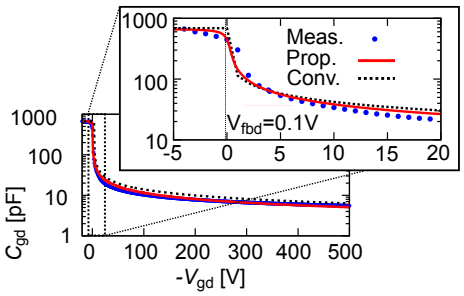

Fig. 2. C_{gd} values from the measurement and the proposed model.

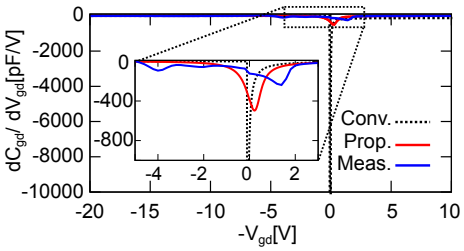

Fig. 3. Derivatives of C_{gd} as functions of V_{gd}.

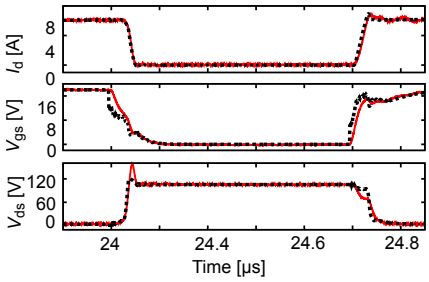

Fig. 4. Measured (solid) and simulated (dashed) waveforms.

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$$\varepsilon_{SiC} E_{SiC} = \sqrt{2q\varepsilon_{SiC} N_D} \sqrt{\phi_t e^{-\phi_{gd}/\phi_t} + \phi_{gd} - \phi_t + e^{-(2\phi_F + V_{ds})/\phi_t} (\phi_t e^{\phi_{gd}/\phi_t} - \phi_{gd} - \phi_t)} \tag{2}$$

$$C_s = \frac{dQ_{gd}}{d\phi_{gd}} = \sqrt{2q\varepsilon_{SiC} N_D} \frac{1 - e^{-\phi_{gd}/\phi_t} + e^{-(2\phi_F + V_{ds})/\phi_t} (e^{\phi_{gd}/\phi_t} - 1)}{2\sqrt{\phi_t e^{-\phi_{gd}/\phi_t} + \phi_{gd} - \phi_t + e^{-(2\phi_F + V_{ds})/\phi_t} (\phi_t e^{\phi_{gd}/\phi_t} - \phi_{gd} - \phi_t)}} \tag{3}$$