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Comparisons of Hot-carrier Effects of Scaled N-Channel and P-Channel Thin-Film SOI Power MOSFETs under Constant Drain Electric Field

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Abstract

This paper compares the hot carrier effect of the n-channel thin-film SOI power MOSFET with that of p-channel one. The device degradation caused by hot carrier effect is promoted by shrinking the design rule despite the constant drain electric field. Hot electrons are injected into gate oxide for n-channel MOSFET. For p-channel one, electrons or holes are injected depending on a stress gate bias condition.

1. Introduction

Power ICs fabricate using SOI technology have become attractive because they can completely isolate the devices each other [1]. The thin-film approach has been promising because of minimizing the parasitic capacitance and reducing thermally induced leakage current.

One of the most important concerns related to the thin-film SOI power MOSFET is how to reduce on-resistance. One of the effective ways to do this is to shrink the channel length. We previously reported the device degradation caused by hot carrier effect under constant electric field for n-channel thin film SOI power MOSFET [2]. In power ICs, both n- and p- channel power MOSFET usually used and detailed analysis have not been reported for p-channel MOSFET.

In this paper, we describe the hot carrier effect of the n-channel power MOSFET and that of p-channel one for scaling the channel length under the constant drain electric field.

2. Device structure and Fabrication process

The schematic cross section of the fabricated thin-film SOI power MOSFET is shown in Fig. 1. The body contacts were formed to suppress the parasitic bipolar effect.

The main structural parameters are listed in Table. 1. The thin-film SOI power MOSFET was fabricated using the 0.5-μm-rule polycide gate process with local oxidation of silicon (LOCOS) isolation. The main device characteristics of n- and p-channel are listed in Table. 2. The electric field is almost the same despite the channel length when the length of the drift region and the same stress bias condition [2].

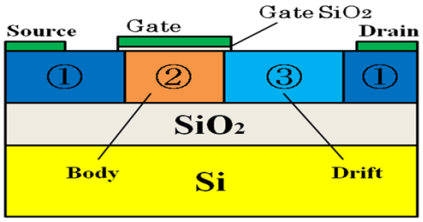

Fig.1 Schematic cross section of SOI power MOSFET
(n-channel:①=n+ ②=p ③=n- p-channel:①=p+ ②=n ③=p-)

Table. 1 The main structural parameter

The name of parameter	Parameter
Top Si layer (μm)	0.14
Buried oxide (μm)	0.4
Gate oxide (nm)	11
Channel Length (μm)	0.5 , 1.0
Drift Length (μm)	0.5

Table.2 The characteristics of the device in this measurement

Channel	n		p	
Channel Length(μm)	0.5	1.0	0.5	1.0
Threshold voltage(V)	0.54	0.55	731	753
On-Resistance(Ω・mm)*	625	867	1731	2612
Break down voltage(V)**	14.0	14.9	12.5	14.8

*Vg=5(V) **Vg=0(V)

3. Result & Discussion

Dependence of threshold voltage shift on the stress gate voltage is shown in Fig. 2. Stress time is 3,600 seconds. Drain voltage is 6V.

$$\text{Threshold voltage shift} = V_{th}(3600s) - V_{th}(0s)$$

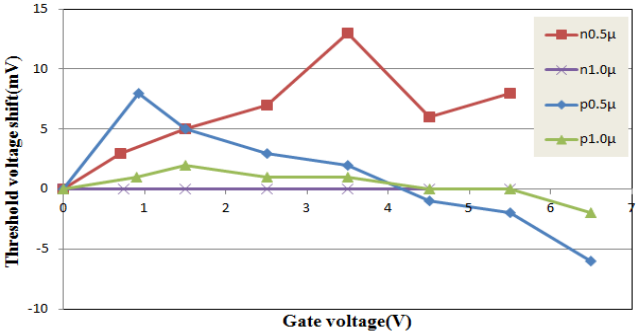

Fig. 2 Threshold voltage shift

For both nMOSFET and pMOSFET, the threshold voltage shift decrease as channel length increases. The threshold voltage shift of the nMOSFET is larger than that of the pMOSFET. For the n-channel power MOSFET, threshold voltage shift increase with increasing gate voltage [2]. For pMOSFET, threshold voltage shift goes plus direction when the gate voltage is more than -4.0V and it goes minus direction when the gate voltage is less than -4.0 V. These results mean that hot electrons are injected into gate oxide when the gate voltage is more than -4V and hot holes are injected into gate oxide when the gate voltage is less than -4V.

When gate voltage is near the threshold voltage, high

electric field appears near the gate edge of the drain junction and electrons which are caused by impact ionization are injected into gate oxide (drain avalanche hot carrier effect)[2]. As gate voltage increase, high electric field appears at the channel region and the majority carriers are injected into gate oxide (channel hot carrier effect).

Dependence of degradation rate of on-resistance on stress gate voltage is shown in Fig. 3. Stress time is 3,600 seconds. Drain voltage is 6V. The detailed figure of Fig. 3 for pMOSFET is shown in Fig. 4.

degradation rate $= R_{on}(3600s)/R_{on}(0s) \times 100 - 100$

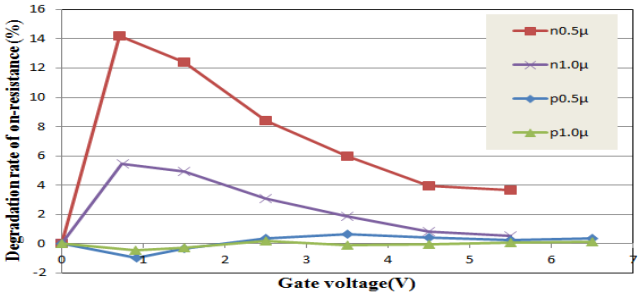

Fig. 3 Degradation rate of on-resistance

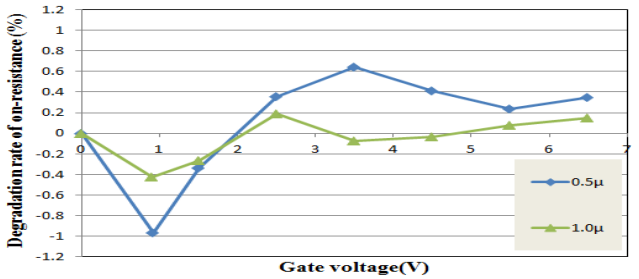

Fig. 4 Detailed figure (pMOSFET)

The degradation rate of the power MOSFET with smaller channel length is larger than that of larger one despite the same electric field. Degradation rate of the nMOSFET is larger than that of pMOSFET. The degradation of the on-resistance has the maximum value near the threshold voltage (Vth + 0.2 V) for the nMOSFET. The degradation rate decreases with increasing the gate voltage. This tendency is similar regardless of the channel length and stress. The degradation rate of the on-resistance is decreased near the threshold voltage for pMOSFET because the gate voltage increases substantially by hot electrons injection. The on-resistance increases with increasing the gate voltage for pMOSFET.

These results means that the hot carrier effect is enhanced by parasitic bipolar effect near the threshold voltage[2].

Dependence of the degradation rate of on-resistance on stress time is shown in Fig.5 (nMOSFET) and Fig. 6 (pMOSFET). Drain voltage is 6V. Gate voltage is Vth+0.2 and 3.5V.

The degradation rate of the on-resistance accelerates at the early stage and degradation rate saturates with the time regardless of the stress gate voltage.

For pMOSFET, the on-resistance decrease near the threshold voltage and it increase at Vg=-3.5V. In the same way as the results of threshold voltage, these results mean hot electrons are injected into gate oxide near the threshold voltage and hot holes are injected into gate oxide at high voltage.

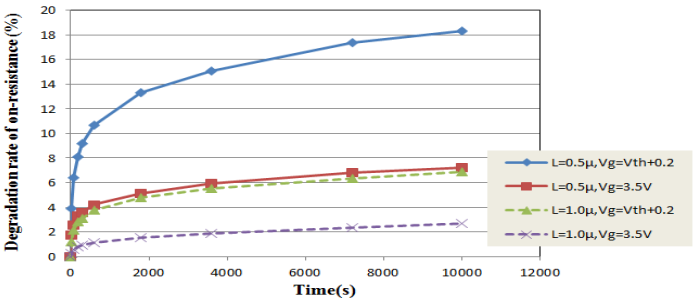

Fig. 5 Degradation rate of on-resistance(nMOSFET)

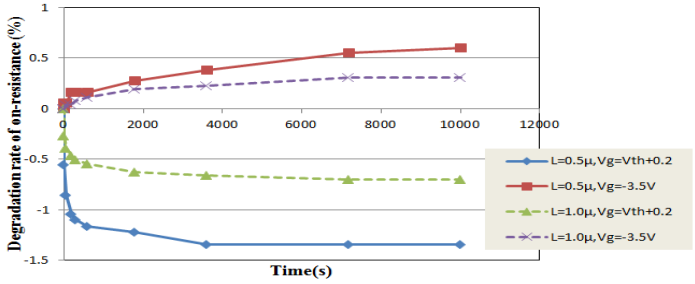

Fig. 6 Degradation rate of on-resistance(pMOSFET)

4. Conclusions

The hot carrier effect of the n-channel power MOSFET and that of p-channel one for scaling the channel length under constant drain electric field has been investigated.

There are two differences between n-channel power MOSFET and p-channel one. One is difference of injected carrier. For n-channel MOSFET, hot electrons are injected. For p-channel MOSFET, hot electrons are injected near the threshold voltage and hot holes are injected under the high gate voltage. The other is device degradation caused by hot carrier effects. Degradation rate of on-resistance for p-channel power MOSFET is smaller than that for n-channel one. For both n and p channel MOSFETs, the hot carrier effects are suppressed by increasing channel length.

Hot carrier effect is enhanced by parasitic bipolar effect near the threshold voltage. Therefore it is necessary to suppress the bipolar effect.

References

[1] J. P. Colinge, Silicon-on-Insulator Technology: Materials to VLSI (Kluwer Academic, Dordrecht, 2004) 3rd ed., p. 4.

[2] T. Takasugi and S. Matsumoto, Jpn. J. Applied Physics, vol.53, No.4, 04EP17,2014.