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4H-SiC bipolar SRAM cell for high temperature applications

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Abstract

Various digital and analog integrated circuits (ICs) have been recently designed and demonstrated using silicon carbide (SiC) bipolar transistors. Though, a memory cell, which is a key component of any electronic system, is yet to be added to the collection of SiC-ICs. This work proposes to bridge that gap and presents the design and analysis of a 4T-SRAM 4H-SiC memory cell capable of stable operation at various temperatures (27 °C-500 °C) with high speeds. The cell uses a 5 V power supply voltage, which is 3 times lower than that used in bipolar 4H-SiC ICs available in the literature. Its good read/write operation capability with fast access times, for a wide range of temperature, confirms the proposed cell compatibility with existing bipolar 4H-SiC ICs and validates its potential in 4H-SiC systems.

1. Introduction

Memory forms a major part of any integrated circuit (IC) and is considered a key component of an electronic system. Over the recent years, the research in silicon carbide (SiC) technology has been geared towards developing bipolar ICs for both digital and analog electronics applications [1] - [5]. These recent advancements calls for developing the missing bipolar memory architecture in order to realize a complete 4H-SiC electronic system.

4H-SiC is a wide bandgap semiconductor with several attractive electrical properties such as low intrinsic carrier concentration and high thermal conductivity, making it suitable for high temperature and high radiation applications.

From the device standpoint, bipolar junction transistors (BJTs) are preferred over metal-oxide semiconductor (MOS) devices for high temperature operation, primarily due to the absence of a critical gate oxide, making oxide reliability a non-issue at high temperatures for a BJT (T > 200 °C) [6].

In this paper, we propose for the first time, the design and analysis of a memory cell, designed using 4H-SiC bipolar technology. This work focuses on the design of static RAM (SRAM) and analysis of its static noise margins (Read and Hold) and access times (Read and Write). To the best of our knowledge, there is no bipolar memory cell based on 4H-SiC present in literature.

2. 4T-SRAM memory cell

A basic SRAM cell can store one-bit in its bi-stable cross coupled inverters. This storage is controlled by the access transistors acting as the cell gates. SRAM cell typically utilizes both npn and pnp transistors in a complementary manner. Due to the low performance of pnp BJTs in 4H-SiC, this study will focus on developing and designing the 4T SRAM cell containing npn BJTs only.

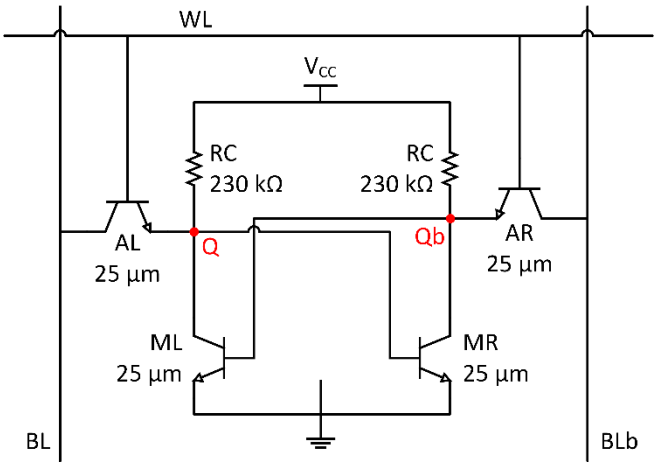

Fig. 1 4H-SiC SRAM circuit diagram consisting of npn transistors and two pull up resistors.

A fully symmetric 4T SRAM cell is depicted in Fig. 1. It has three main states: read, write, and hold. To briefly explain its working, the bitlines are first pre-charged to V_{CC}, before reading, and the cell is accessed through A_L and A_R by asserting the *WL* line. The values inside the cell (*Q*/*Qb*) are then reflected in the bitlines, completing the read operation. This process is inverted for the write operation where the memory state is influenced by the bitlines. The bitlines are preconnected to complementary levels (V_{CC} and *GND*) before the cell is accessed. Finally, the data is held by setting *WL* to *GND*, which causes the cell to latch the data in the cross-coupled inverters, as long as power is supplied [7].

The simulations use the transistor discussed in [2], and has the following properties at room temperature: current gain of 56, cutoff frequency of 1.4 GHz, and a $V_{BE,ON}$ of around 2.8 V. The effect of temperature is accounted for by using different transistor models for each temperature and accounting for resistivity changes for the resistors.

SPICE simulations are used to optimize the circuit parameters. The correct functionality of the SRAM cell requires appropriate relative sizing of the transistors, keeping in mind the performance tradeoffs. For example, making the memory transistors (M_R and M_L) bigger than access transistors (A_R and

A_L) makes it harder to change the cell's state, which is beneficial for a stable read operation, but adversely affects the writing speed. Additionally, sizing the resistors (*RC*s) should address the trade-off between cell size and correct functionality. An additional constraint for this work is that the design should be robust enough to sustain high temperatures. Keeping these constraints in mind, the optimized design of the 4H-SiC 4T-SRAM cell has all transistors sized at 25 µm and the value of *RC* is set to 230 kΩ.

3. Performance evaluation

The performance of an SRAM cell can primarily be determined by cell stability and speed. A stable SRAM cell should successfully retain its stored data during the hold and read states. The cell stability is measured by hold and read static noise margins (SNMs) which are evaluated while *WL* is kept low, and high, respectively, which makes the read SNM different than hold SNM. The hold SNM and read SNM exhibited by the optimized cell at room temperature are 2.25 V and 1.25 V, respectively. Fig. 2 shows that the SNM values are acceptable for maintaining cell functionality at all temperatures. The degradation of the SNMs at higher temperatures is attributed to the decrease in $V_{BE,ON}$, V_{CE} and the change in resistor values with increasing temperature, as discussed in [3].

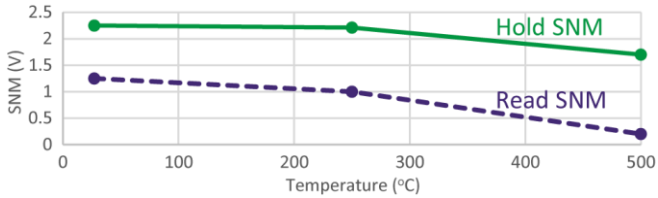

Fig. 2 Read and hold SNM values of 4H-SiC SRAM at different temperatures.

The speed of the SRAM cell is evaluated during both read and write operations. The rise/fall times of controlled signals, like *WL*, are set to 300 ps, and the wire capacitance and other parasitics are simulated as 1 pF for this work. Read time is defined as the time needed to read the stored bit from the cell. It is measured as the time difference between asserting WL and reaching 10% V_{CC} voltage difference between the bitlines [8]. The cell demonstrates a read time of 1.9 ns at room temperature which increases to 2.5 ns at 500 °C. This is attributed to the fact that both 4H-SiC BJT's current gain and speed decrease, while the 4H-SiC resistors' resistivity increases, with increasing temperature.

The speed of the write operation can be defined and characterized using four different parameters: 1) Write time: the time delay required for the cell to change its state, 2) Settling time: the time needed for the new values to stabilize during a write operation, 3) Setup time: the time for which the bitlines must be preset prior to asserting *WL* for write operation, and 4) *WL* pulse width: the time period required for *WL* to stay high during cell access. The values of all mentioned timing parameters at different temperatures are laid out in Table I. It is clear from the table that the required setup time decreases as temperature increases, until it is not required at 500 °C. The table also shows that cell writing (minimum WL pulse width, minimum setup time, and write time) is faster as the temperature increases. This is in corroboration with the SNM results as the cell is easier to write to, at higher temperatures. Finally, it is observed that the setup time and WL pulse width are related in such a way that setting one of them to more than its minimum value, relaxes the required minimum value of the other, while maintaining correct write operation.

Table. 1 Read and write timing parameters for the optimized 4H-SiC 4T-SRAM cell at different temperatures

Temp. (°C)	Read time (ns)	Min. WL pulse width (ns)	Min. Setup time (ns)	Write time (ns)	Worst case settling time (ns)
27	1.93	124.00	5.00	84.01	215.31
250	2.07	25.00	3.50	11.35	132.73
500	2.54	12.20	0.00	4.00	91.81

4. Conclusions

In this work, a 4H-SiC SRAM cell that is capable of operating at temperatures up to 500 °C is presented. The cell shows stable performance across wide range of temperatures with good speeds. It exhibits hold/read SNMs of 2.25 V/1.25 V at room temperature and maintains non-zero hold/read SNMs of 1.7 V/0.2 V at 500 °C, respectively. The obtained results demonstrate the potential of memory architectures in 4H-SiC for small-scale logic applications.

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