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Poly-InSb nMOSFETs for monolithic 3DIC

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Abstract

Poly-InSb films have been investigated as 3DIC channel materials. Rapid thermal annealing (RTA) method was utilized to form poly-InSb films from amorphous InSb films (a-InSb) by thermal crystallization. High Hall electron mobility of 432 cm^2/Vs has been achieved, which is higher than that of Si. Poly-InSb nMOSFETs with the channel thickness of only 5 nm were also successfully demonstrated, showing an on/off ratio of 20.

Introduction

In order to realize monolithically 3D integration, poly-crystalline semiconductors on insulator layers are considered suitable for channel materials of FET complying with the thermal-budget constraints. High-quality poly-crystalline Ge (poly-Ge) pMOSFETs have already been demonstrated, and the device performance is comparable to that of c-Si pMOSFETs. However, nMOSFETs with poly-crystalline semiconductors have not well-developed yet. InSb owns the highest electron mobility among the III-V based semiconductor. Therefore, InSb channel with the quantum well structure FET [1] and with Al_2O_3/InSb gate stack [2] have been examined as future scaled FETs. Furthermore, thick poly-InSb film (1.7 μm) has been proven to present high Hall mobility of 6500cm^2/Vs [3], which shows poly-InSb is a promising candidate as nMOSFETs channel materials. In this work, we examine the feasibility of poly-InSb channel for future 3DIC

Experiment

Figure 1 shows the process flow for fabricating poly-InSb thin films on Si. First, a 100-nm-thick a-InSb layer was deposited by RF sputtering on a 600-nm-thick SiO_2 layer. RTA was then carried out for crystallization of the a-InSb film in a nitrogen atmosphere at the annealing temperature from 100 to 550℃ for 30 minutes. To evaluate the poly-InSb crystal quality and electrical characteristics, atomic force microscopy (AFM), cross-sectional scanning electron microscopy (SEM), and Hall effect measurements were performed.

Figure 2 shows a schematic device structure and the fabrication flow of front-gate poly-InSb nMOSFETs. A 20-nm-thick SiO_2 gate dielectric layer and a 30-nm-thick TaN metal gate layer were deposited by sputtering. After gate patterning, RTA for InSb crystallization was carried out. Then, SiO_2 in source/drain areas were removed by RIE.

Results and discussion

Figure 3 shows XRD 2θ scan spectrum of InSb thin films before and after RTA. XRD peaks corresponding to InSb (111), InSb (220), and InSb (311) were detected after RTA at the temperature more than 300℃. a-InSb can be crystallized by a simple thermal method and the crystalline quality improves as increasing RTA temperature. Since In metal peaks were also observed, it was important to adjust the chemical composition in InSb films in binary alloy. Figure 4 shows the AFM images of the InSb surface before and after annealing. A surface roughness of a-InSb before annealing is Rms = 0.2-nm, but a surface roughness of poly-InSb after annealing increased to Rms = 14-nm. The grain size of the poly-InSb layer after annealing was found to be 50~500 nm, which can be applied to make a poly-InSb FETs. Figure 5 shows cross-sectional SEM images of the InSb thin film before and after annealing. Surface of a-InSb film and interface of InSb/SiO_2 are very smooth, but, roughness in InSb surface after anneal at 500 ℃ increased and voids formed during the poly crystallization. Figure 6 plots the electron Hall mobility as a function of carrier density. As increasing RTA temperature, higher electron mobility is obtained from poly-InSb thin films. In spite of surface roughening and void formation, the electron mobility of 432 cm^2/Vs was attained, that is larger than that of Si.

We further investigated the device performance of deletion-type poly-InSb MOSFETs. In order to suppress the surface roughness of InSb layer as well as to form a gate dielectric layer, a 20-nm-thick SiO_2 cap layer was implemented for MOSFET fabrication. Also, in order to deplete the carrier completely, the channel thicknesses ($T_{channel}$) were limited to 20 and 5nm, respectively. Figure 7 shows Id-Vg characteristics of poly-InSb nMOSFETs. We found the drain current modulation by changes in the gate voltage to obtain on/off ratio of 4 for $T_{channel}$ of 20nm. On the other hand, on/off ratio was improved to 20 by thinning the channel thickness to 5 nm. While the off current was successfully reduced by a factor of 100, on-current also degraded to 1/50. The cause of the on-current deterioration is attributed to a parasitic resistance of the source and the drain part due to the ultra thin body. We verified the material potential of poly-InSb film as a channel in MOSFET.

Conclusion

High Hall electron mobility of up to 432 cm^2/Vs for poly-InSb layers on insulator layers were obtained by the RTA process. The mobility values were higher than that of c-Si with the same carrier density. We fabricated poly-InSb nMOSFETs successfully for the first time. These results suggest that the poly-InSb nMOSFETs have great potential for future 3DIC.

References

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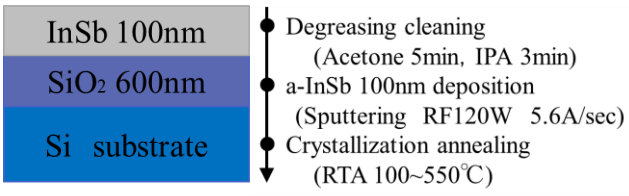


Fig.1 Schematic structure and process flow for fabricating poly-InSb thin films on Si.

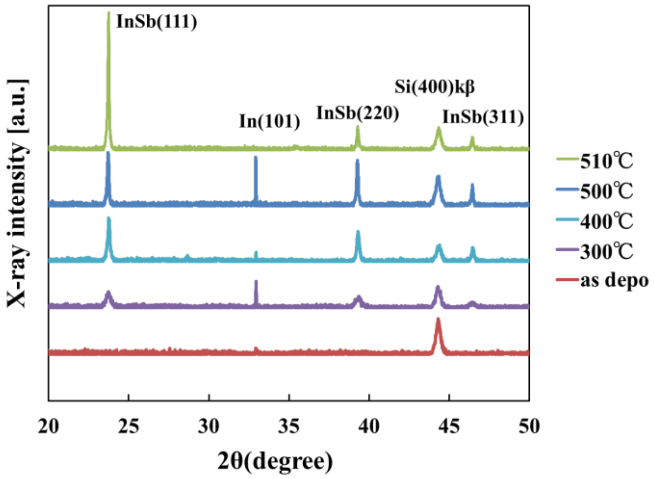


Fig.3 XRD 2θ scan of as deposited amorphous InSb, and poly-InSb formed by RTA annealing at different temperatures

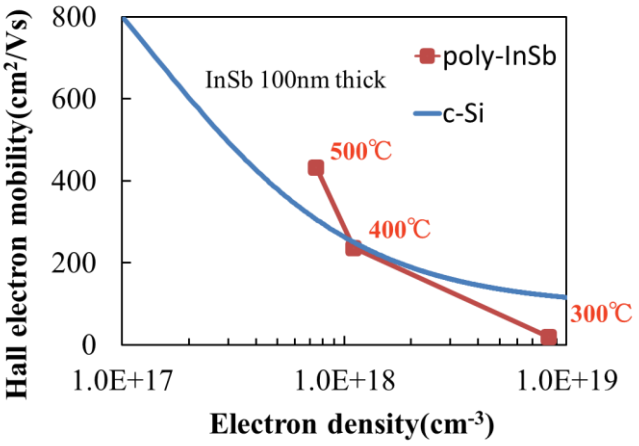
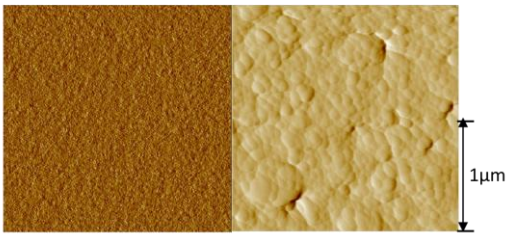
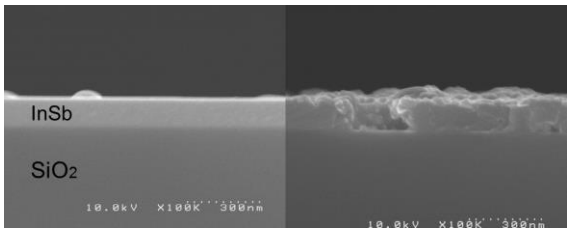


Fig.6 Hall electron mobility of 100-nm-thick poly-InSb.



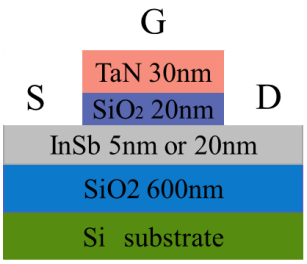
Before aneal After aneal

Fig.4 AFM images of InSb surface before and after thermal annealing. (500℃, 30min)



Before aneal After aneal

Fig.5 Cross-sectional SEM images of InSb film before and after annealing. (500℃, 30min)



- SiO2 (600nm) on (100)Si substrate
- InSb (5nm or 20nm) & SiO2 (20nm) depo. (sputter)
- TaN (30nm) depo. (sputter)
- Gate patterning. (RIE)
- InSb crystallization RTA (400℃, 1min)
- SiO2 on InSb remove. (RIE)

Fig.2 Schematic device structure and the process flow of poly-InSb nMOSFETs

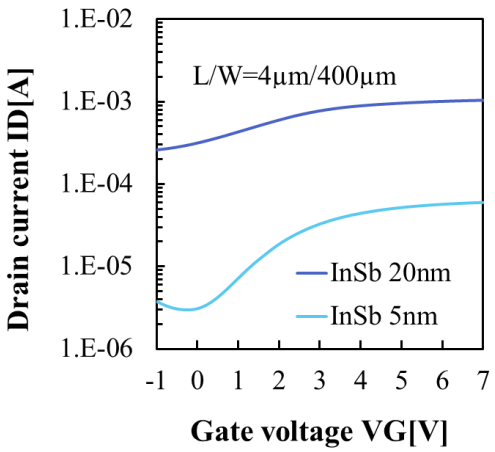


Fig.7 Id-Vg characteristics of FLA poly-InSb nMOSFETs