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Novel Integrated Voltage Regulators with High-Side NMOS Power Switch and Dedicated Bootstrap Driver Using Vertical MOSFET for Efficiency Enhancement

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Abstract

In this paper, we propose novel Integrated Voltage Regulators (IVR) with cascode bridge composed of High-Side (HS) NMOS power switch and dedicated bootstrap driver for improving efficiency. Power switching of twice process voltage V_{MAX} with NMOS HS power switch is realized by novel circuit technique that directly connects bootstrap pin to the gate of input-voltage-side NMOS. Moreover, by using vertical MOSFET free from Back Bias (BB) effect, on-resistance increase of HS NMOS power switch due to high input voltage is significantly suppressed, and drain-to-source voltage of MOSFETs in off-state is distributed uniformly in comparison with planar MOSFET. Proposed IVR with 3.3 V input voltage and 1.2 V output voltage is designed and simulated by HSPICE. Efficiency of the proposed IVR is 84% at peak and 81 % at heavy load of 2 A, which is 3% and 11% higher than conventional IVR with HS PMOS power switch in same transistor size.

1. Introduction

Designing voltage regulator with higher switching frequency minimizes the size of passive components such as inductor and decoupling capacitor. To achieve very high switching frequency such as 100 MHz, IVR implemented in low voltage CMOS technology has been developed [1,2]. To support large input voltage above CMOS process voltage V_{MAX}, cascode bridge that several MOSFETs are connected in series is applied for power stage. In previous works, PMOS is applied for HS power switch as shown in Fig. 1. It is issue that large on-resistance of PMOS severely degrades efficiency of IVR. However, NMOS cannot be applied HS power switch due to its BB effect (See Section 3). In this paper, novel cascode bridge composed of Vertical (V) NMOS HS power switch is proposed and simulated with 0.18 μm vertical MOSFET which has excellent performance for power switch.

2. Concept of the Proposed Circuit

Fig. 2 shows the proposed circuit with Vertical MOSFET and its HS NMOS power switch. Passive components such as inductor, decoupling capacitor, and bootstrap capacitor are implemented on package which is similar to conventional IVR. In the proposed circuit, two V-NMOS in series (M1, M2) are used as HS power switch. Input voltages are V_{in} and V_{hr} that is a half voltage of V_{in}. To drive HS V-NMOS power switch, bootstrap driver is applied. M5 and M6 are connected in series to handle twice process voltage. They turn on when switching node goes low like a bootstrap diode. The timing diagram of the proposed HS V-NMOS power switch and bootstrap driver is shown in Fig. 3. It should be noted that bootstrap pin is directly tied to the gate of M1. Voltage of bootstrap pin V_{BST} swings from V_{hr} to (V_{IN}+V_{hr}), accordingly V_{gs} of M1 is kept to V_{hr} like V_{gs} of M3 of low-side power switch. Hence, simple circuit design without gate loss can be achieved because M1 is driven without additional driver.

3. Advantages of Vertical MOSFET for Power Switch

In Fig. 4 (a), voltages of important terminals when HS NMOS power switch is on-state are described. Switching node voltage V_{SW} becomes approximately the same as V_{IN}, which means extremely large negative BB voltage is applied in M1 and M2 as shown in Fig. 4 (b). Therefore, using planar NMOS for HS power switch has a difficulty because triple-well process option was necessary to control BB voltage in conventional approach [3]. We propose to use Vertical NMOS to HS power switch as shown in Fig. 5 for its BB free characteristics [4,5], as its channel is separated from the substrate. Fig. 6 shows the V-MOSFET is fully depleted so that its threshold voltage increase is completely neglected. Output current comparison between NMOS and PMOS of planar and V-MOSFET for HS power switch is shown in Fig. 7. It is obvious that proposed V-NMOS can draw much larger output current than conventional planar PMOS. Moreover, by using V-MOSFET, voltage distribution of two MOSFETs in off-state becomes more uniform than planar MOSFET shown in Fig. 8. It indicates that higher voltage power switching in same process voltage can be achieved with Vertical MOSFET.

4. Simulation Results and Discussions

The simulated parameters of IVR are summarized in Table 1. Simulated waveform of the proposed circuit is shown in Fig. 9. The 3.3 V swing of switching node (SW) indicates that our proposed direct connection from bootstrap pin to M1 gate successfully drives the HS NMOS power switch. Efficiency comparison between proposed and conventional IVR is shown in Fig. 10. The proposed IVR and conventional IVR with PMOS HS power switch is compared with the same transistor size L/W. The peak efficiency of the proposed IVR is 84%, which is 3% higher efficiency than conventional IVR, in other words, 16% loss reduction is achieved. In heavy load region at 2A load current, efficiency improvement of the proposed IVR is 11%. In Fig. 11, loss in power transistors M1 - M4 at 0.5A load current is shown. Because of higher mobility of Vertical NMOS without BB effect than PMOS, the loss in M1 and M2 is significantly suppressed as much as 43% and 46% respectively.

5. Conclusions

Novel IVR with cascode bridge composed of HS Vertical NMOS power switch and bootstrap driver was proposed, which achieved much higher efficiency than conventional IVR. Moreover, excellent performance of V-MOSFET for power switch both in on-state and off-state is clarified.

Acknowledgements

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References

[1] G. Schrom et al., APEC, CA, pp. 727-730, 2010.

[2] E. A. Burton et al., APEC, TX, pp. 432-439, 2014.

[3] C. Huang et al., ISCAS, Beijing, pp. 693-696, 2013.

[4] T. Endoh et al., IEEE ED 50, 945, 2003.

[5] K. Sakui et al., Solid-State Electronics, vol. 54, issue 10, pp. 1192-1196, Oct. 2010.

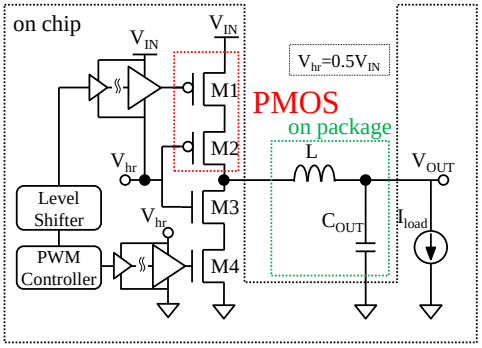

Fig. 1 Block diagram of conventional IVR with cascode bridge composed of HS PMOS power switch.

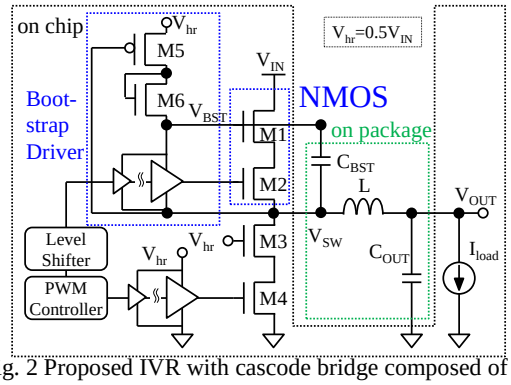

Fig. 2 Proposed IVR with cascode bridge composed of HS NMOS power switch and dedicated bootstrap driver.

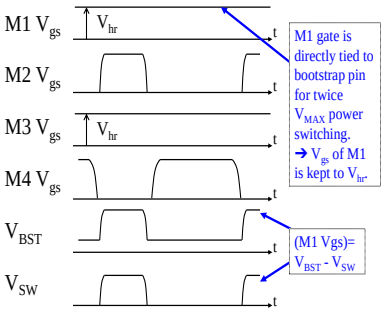

Fig. 3 Timing diagram of the proposed bootstrap driver for cascode bridge composed of HS NMOS power switch.

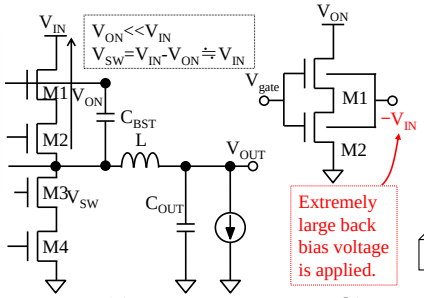

Fig. 4 (a) Voltage of terminals and (b) equivalent bias condition of HS NMOS power switch when on-state.

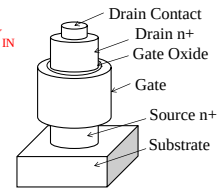

Fig. 5 Vertical MOSFET structure.

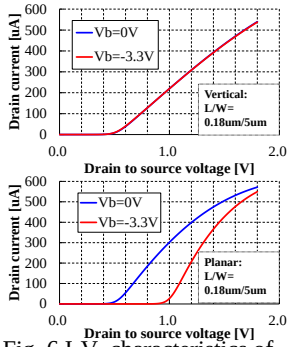

Fig. 6 I_dV_g characteristics of vertical MOSFET comparison with planar MOSFET.

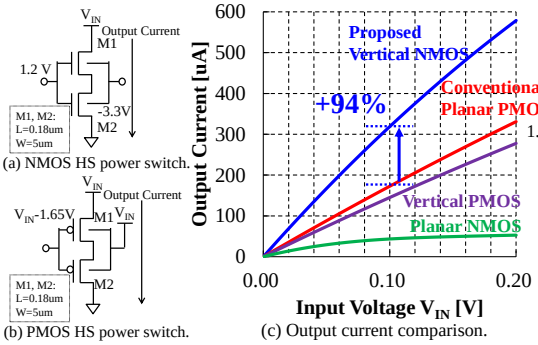

Fig. 7 Output current comparison between NMOS and PMOS of planar and vertical MOSFET for HS power switch assumption.

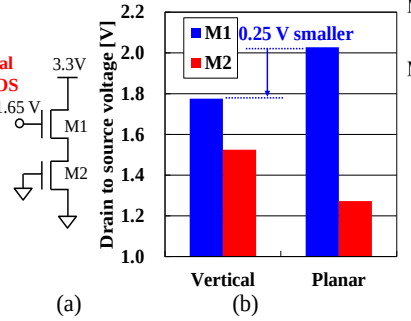

Fig. 8 (a) NMOS power switch in off-state and (b) comparison of voltage distribution between vertical and planar MOSFET.

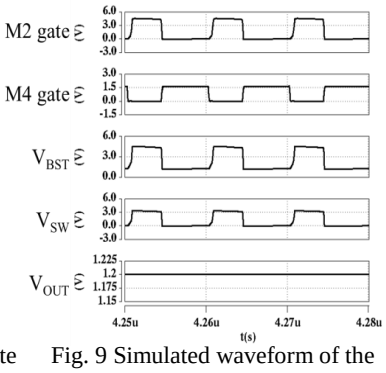

Fig. 9 Simulated waveform of the proposed IVR under load current is 0.5 A.

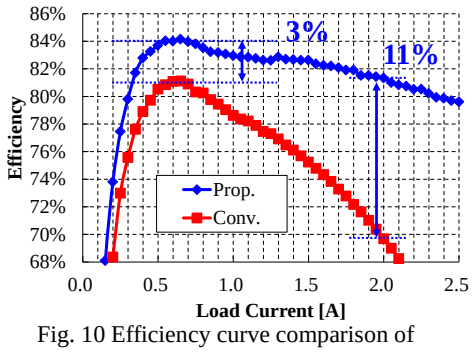

Fig. 10 Efficiency curve comparison of the proposed and conventional IVR.

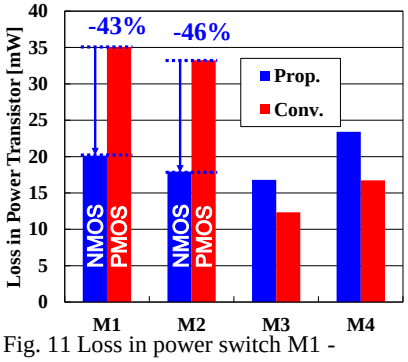

Fig. 11 Loss in power switch M1 - M4 under load current is 0.5 A.

Table 1 Parameters of the simulated IVR.

Input voltage V_{IN}	3.3 V
Input voltage V_{hr}	1.65 V
Output voltage V_{OUT}	1.2 V
Inductance	4 nH
Output capacitance	10 uF
Bootstrap capacitance	4.5 nF
Crossover frequency	10 MHz
Switching frequency	100 MHz
MOSFET Models	BSIM4 0.18um vertical MOSFET model extracted from experimental data