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Multi-Ring MOSFETs for Mobility Enhancement and Parasitic Resistances Reduction in RF and Analog Applications

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Abstract

Multi-ring (MR) devices are designed and implemented in 90 nm RF CMOS process for transconductance (g_m) enhancement and gate resistance (R_g) reduction, which are the key factors for RF and analog performance improvement. Under the condition of the same finger width and total channel width, the MR n-MOSFETs can achieve around 7% higher g_m and 10% smaller R_g than multi-finger (MF) n-MOSFET. The increase of g_m is attributed to higher effective mobility (μ_{eff}) and smaller source resistance (R_S). The former proves the success of MR layout for reduced STI stress and the latter accounts for an effective reduction of the source line and contact resistances. The MR devices yielding the mentioned advantages becomes an attractive option for RF and analog design.

I. Introduction

MF devices have been widely used in RF and analog circuits for R_g reduction to reach higher f_{MAX} and lower noise [1]-[3]. Unfortunately, the MF layout with larger finger number (N_F) and smaller finger width (W_F) may lead to the penalties like lower μ_{eff} due to increased STI transverse tress ($\sigma_\perp$) and larger R_S from longer source line. Both of which result in g_m degradation and negative impact on f_T, f_{MAX}, and RF noise. Donut devices, both n- and p-MOSFETs implemented in our previous work were proven successful to eliminate the STI $\sigma_\perp$ and achieve higher μ_{eff} as well as improvement of g_m and f_T [4]. However, the donut devices with poly-gate in a single ring generally suffer much larger R_g and undesired degradation like lower f_{MAX} and higher RF noise. In this paper, MR devices with the poly-gate in the multiple rings layout are proposed to effectively reduce R_g and maintain the advantages of μ_{eff} and g_m. MR and MF devices are fabricated on the same chip in 90 nm RF CMOS process to realize a fair comparison based on nearly the same process parameters.

II. MF and MR Devices - Layout and Basic Parameters

Fig.1(a)~(c) illustrate MF and single-ring (donut) device layouts in which $\sigma_{//}$ and $\sigma_\perp$ denote the longitudinal and transverse stress. For MF devices (Fig.1(a)) with $W_F \times N_F$ =2 μm×16, 1μm×32, and 0.5 μm×64, the smaller W_F associated with larger N_F will increase $\sigma_\perp$ and lead to lower μ_{eff} owing to the compressive $\sigma_\perp$ from STI [4]. As for the single-ring devices (Fig.1(b),(c)), the compressive $\sigma_\perp$ can be eliminated but $\sigma_{//}$ remains there, responsible for μ_{eff} degradation in n-MOSFETs. Thus, the single-ring layout with enlarged length of active region (LOD) is proposed to reduce $\sigma_{//}$. Herein, D1S1 (Fig.1(b)) denotes the typical rule, given by LOD=0.36μm and 0.45μm, corresponding to S_{DOD}=0.16μm and S_{SOD}=0.25μm at drain and source sides. D1S3 (Fig.1(c)) is specified with 3 time larger S_{SOD} to 0.75μm, yielding LOD=0.95μm at the source sides. The enlarged LOD intends to effectively reduce $\sigma_{//}$ and recover μ_{eff}. Taking the single-ring layout as the template, MR devices shown in Fig.2, with 4 rings and different LOD, namely W2N4R4_D1S1 and W2N4R4_D1S3 are designed, given with W_F =2μm, R=4, and N_F=4×R=16. Also, MR devices with 8 rings can be implemented with W_F =1μm, R=8, and N_F=4×R=32. Note that MF and MR devices follow the layout splits with fixed total width, $W_{tot}=W_F \times N_F$=32μm. Table 1 summarizes the basic device parameters extracted by using our proprietary device parameters extraction method [5]-[6] in which L_g, $T_{ox(inv)}$ or $C_{ox(inv)}$ and ΔW are necessary for μ_{eff} extraction. Besides, the parasitic resistance R_S is another key parameter to be known for an accurate μ_{eff} extraction from the measured I-V characteristics. Fig. 3 shows the R_S determined by our transmission line (TML) model [7] for MF and MR devices. The results indicate an approximately linear increase of R_S versus N_F and the MR devices can achieve around 16~30% smaller R_S than MF devices with the same W_F and N_F. The reduction of R_S is an important factor beside the μ_{eff} enhancement for g_m improvement.

III. Comparison of MR and MF Devices – g_m, μ_{eff}, and R_g

In the following, a serious comparison between the MR and MF n-MOSFETs will be focused on three major device parameters, g_m, μ_{eff}, and R_g, which are key factors responsible for the RF and analog performance, such as f_T, f_{MAX}, and RF noise. According to the analytical models expressed by (1)~(3) [8]-[9], g_m is the most important parameter with direct and significant influence on f_T, f_{MAX}, and minimum noise figure (NF_{min}). Furthermore, R_g has major impact on f_{MAX}, NF_{min}, and equivalent noise resistance (R_n) given by (2)~(4) [8].

$$f_T = \frac{g_m}{2\pi\sqrt{C_{gg}^2 - C_{gd}^2}} \quad (1)$$

$$f_{MAX} = \frac{f_T}{2\sqrt{R_g(g_{ds} + 2\pi f_T C_{gd}) + g_{ds}(R_i + R_s)}} \quad (2)$$

$$F_{\min} = 1 + \kappa \frac{f}{f_T}\sqrt{g_m\left(R_g + R_S\right)} \quad (3)$$

$$NF_{\min} = 10\ell og\left(F_{\min}\right)$$

$$R_n \approx R_g + \gamma\frac{g_{do}}{g_m^2}\ (\gamma > 1\ \textit{for short channel}) \quad (4)$$

where, C_{gd} and C_{gg} represent the gate to drain capacitance, and total gate capacitance, which can be determined from the intrinsic Y-parameters after a dedicated open and short deembedding to the bottom metal layer, i.e. metal-1[8].

First, Fig. 4 (a) shows the g_m versus V_{GT} measured from the MF and MR n-MOSFETs in linear region (V_{DS}=50mV). Note that V_{GT}=(V_{GS}-V_T) is used to offset the V_T variations between the devices with different layouts for a fair comparison. The results indicate that W1N32 with the smaller W_F and larger N_F in the MF layout suffers the lowest g_m, which reveals around 6% degradation compared to W2N16 and suggests the impact from STI $\sigma_\perp$ on μ_{eff} and longer source line on R_S. On the other hand, W2N4R4_D1S3 in the MR layout can offer the largest g_m, which is around 5% higher than W2N16 and 11% higher than W1N32. Then, taking MF devices as the reference, Fig. 4 (b) shows the increase of g_m realized by MR devices compared with the reference with the same W_F and N_F, and normalized to the reference, denoted as $\Delta g_m/g_{m(MF)}$. The results indicate that W1N4R8_D1S1 can yield

5~7.2% higher g_m than W1N32. However, the $\Delta g_m/g_{m(MF)}$ achieved by W2N4R4_D1S1 w.r.t. W2N16 is below 3.6% and the $\Delta g_m/g_{m(MF}$ can be increased to around 6% by W2N4R4_D1S3 with enlarged LOD, attributed to reduced STI $\sigma_{//}$. Furthermore, the μ_{eff} can be extracted from the linear I-V model given by (5) in which the basic device parameters like L_g, $C_{ox(inv)}$, and W_{eff} can be known from Table 1, determined by using our proprietary method [5]-[6] and the measured $I_{DS}(V_{GT}, V_{DS})$. Fig.5 (a) and (b) show the μ_{eff} versus V_{GT}, extracted from the MF and MR n-MOSFETs with W_F=2μm and 1μm, respectively. The comparison of W2N4R4_D1S3 versus W2N16 and W1N4R8_D1S1 versus W1N32 indicates that the MR devices can achieve apparently higher μ_{eff} than the MF devices with the same W_F and N_F. The results prove that the MR layout with eliminated STI $\sigma_{\perp}$ and reduced STI $\sigma_{//}$ from the enlarged LOD can contribute higher μ_{eff}. Finally, Fig. 6 presents the R_g determined by using Y-method, according to (6) [8]. The results indicate a significant R_g reduction when increasing N_F and around 10% lower R_g in the MR devices than MF devices with the same W_F and N_F. It means that the MR devices can simultaneously yield higher g_m and lower R_g.

$$\mu_{eff} = \frac{L_g}{W_{eff} C_{ox(inv)}} \cdot \frac{I_{DS}}{(V_{GS} - V_T - \lambda V_{DS})(V_{DS} - I_{DS} \cdot R_S)}, \; 0 < \lambda \le \frac{1}{2} \quad (5)$$

$$W_{eff} = (W_F + \Delta W) \cdot N_F$$

$$R_g = \mathrm{Re}(Y_{11}) / \left[\mathrm{Im}(Y_{11})\right]^2 \quad (6)$$

IV. Conclusion

The MR devices realized by 90nm RF CMOS process have been proven successful with significant g_m enhancement over the MF devices, attributed to simultaneous improvement of μ_{eff} and R_S. Moreover, the MR devices can yield 10% smaller R_g. The higher g_m and lower R_g can contribute higher f_T and f_{MAX} as well as lower NF_{min} and R_n. These important features can facilitate RF and analog performance optimization.

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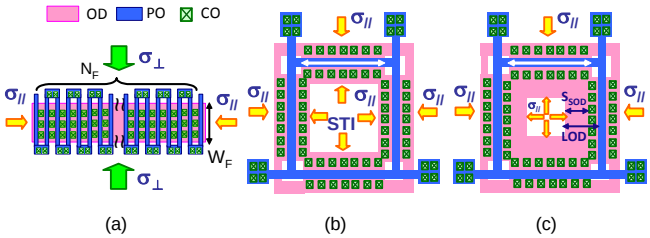

Fig. 1 Schematics of device layouts (a) MF devices with various W_F and N_F at fixed $W_{tot}=W_F x N_F$ (b) single-ring device D1S1 : LOD/ S_{DOD}=0.36μm /0.16μm, LOD/S_{SOD}=0.45μm/0.25μm (c) single-ring device D1S3 : LOD/ S_{DOD}=0.36μm/0.16μm,LOD/S_{SOD}=0.95μm/0.75μm. S_{DOD} and S_{SOD} : drain and source OD edge to the contact spaces. OD : active region, PO : poly-gate, CO : contacts.

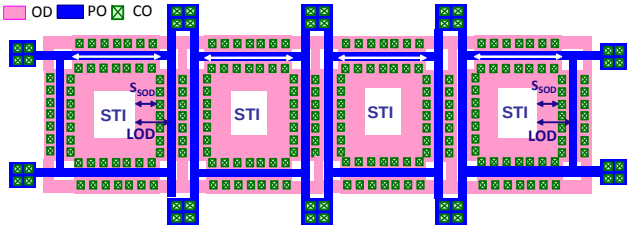

Fig.2 Multi-ring MOSFET layouts : W2N4R4 with 4 rings (R=4), W_F =2μm, N_F=4, in each ring, W1N4R8 with 8 rings (R=8), W_F=1μm, N_F =4 in each ring. D1S1 : S_{DOD}=0.16μm, S_{SOD}=0.25μm, D1S3 : S_{DOD}=0.16μm, S_{SOD}=0.75μm. OD : active region, PO : poly-gate, CO : contacts.

Table 1 The device parameters of MF and MR nMOSFETs

Parameters	Unit	MF & MR devices
L_g	μm	0.077
$T_{ox(inv)}$	A	28.3
$C_{ox(inv)}$	fF/μm^2	12.2016
$C_{of,sim}$	fF/μm	0.26303
$C_{f(poly-end),sim}$	fF	0.05015
$C_{ox(inv)}$ =(β/$W_F N_F$ - C_{of})/L_g	fF/μm^2	12.2016
$T_{ox(inv)}=\varepsilon_0\varepsilon_{ox}/C_{ox(inv)}$	A	28.3
$\Delta W=(\alpha-C_{f(poly-end)})/(C_{ox(inv)}L_g)$	μm	0.0348

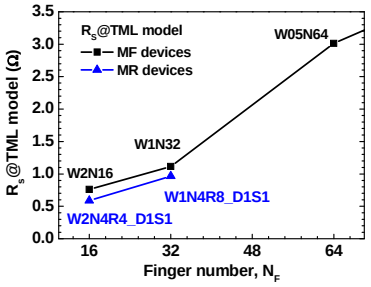

Fig.3 Comparison of R_S versus N_F calculated by TML model for MF and

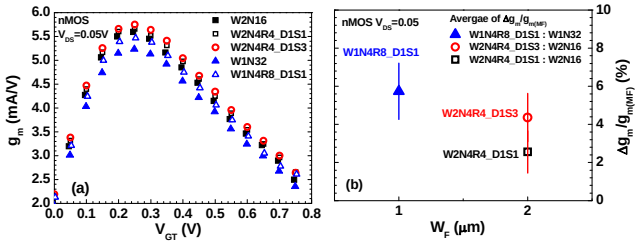

Fig 4 Comparison of MF and MR MOSFETs (a) g_m versus V_{GT} in linear region (V_{DS} =50 mV) (b) $\Delta g_m/g_{m(MF)}$ versus W_F of MR w.r.t MF MOSFETs. MR MOSFETs with various W_F and N_F.

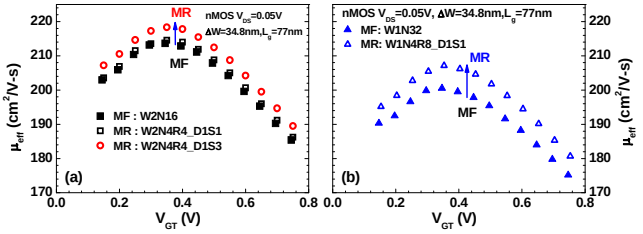

Fig. 5 Comparison of μ_{eff} versus V_{GT} extracted from MR and MF MOSFETs in linear region, V_{DS} =50mV (a) W2N16, W2N4R4_D1S1, W2N4R4_D1S3 (b) W1N32, W1N4R8_D1S1.

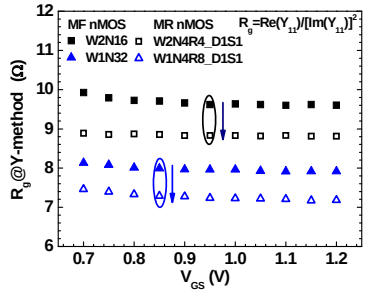

Fig.6 R_g extracted by Y-method at cold device state (V_{DS}=0, V_{GS} > V_T) for MF and MR devices, MF devices : W2N16 and W1N32, MR devices : W2N4R4_D1S1 and W1N4R8_D1S1.

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