Multi-Ring MOSFETs for Mobility Enhancement and Parasitic Resistances Reduction in RF and Analog Applications

Yen-Ying Lin and Jyh-Chyurn Guo
Institute of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan
Tel: +886-3-5131368, Fax: +886-3-5724361, E-mail: jeguo@mail.nctu.edu.tw

Abstract

Multi-ring (MR) devices are designed and implemented in 90 nm RF CMOS process for transconductance ($g_m$) enhancement and gate resistance ($R_g$) reduction, which are the key factors for RF and analog performance improvement. Under the condition of the same finger width and total channel width, the MR n-MOSFETs can achieve around 7% higher $g_m$ and 10% smaller $R_g$ than multi-finger (MF) n-MOSFET. The increase of $g_m$ is attributed to (Fig.1(c)) is specified with 3 times larger $SSOD$ to 0.75 single-ring layout with enlarged length of active region ($LOD$) is $LOD=0.95$ of the former proves the success of MR layout for reduced STI stress and the latter accounts for an effective reduction of the source line and contact resistances. The MR devices yielding the mentioned advantages becomes an attractive option for RF and analog design.

I. Introduction

MF devices have been widely used in RF and analog circuits for $R_g$ reduction to reach higher $f_{MAX}$ and lower noise [1]-[3]. Unfortunately, the MF layout with larger finger number ($N_F$) and smaller finger width ($W_F$) may lead to the penalties like lower $\mu_{eff}$ due to increased STI transverse stress ($\sigma_{//}$) and larger $R_g$ from longer source line. Both of which result in $g_m$ degradation and negative impact on $f_T$, $f_{MAX}$ and RF noise. Donut devices, both n- and p-MOSFETs implemented in our previous work were proven successful to eliminate the STI $\sigma_{//}$ and achieve higher $\mu_{eff}$ as well as improvement of $g_m$ and $f_T$ [4]. However, the donut devices with poly-gate in a single ring generally suffer much larger $R_g$ and undesired degradation like lower $f_{MAX}$ and higher RF noise. In this paper, MR devices with the poly-gate in the multiple rings layout are proposed to effectively reduce $R_g$ and maintain the advantages of $\mu_{eff}$ and $g_m$. MR and MF devices are fabricated on the same chip in 90 nm RF CMOS process to realize a fair comparison based on nearly the same process parameters.

II. MF and MR Devices - Layout and Basic Parameters

Fig.1(a)-(c) illustrate MF and single-ring (donut) device layouts in which $\sigma_{//}$ and $\sigma_{\perp}$ denote the longitudinal and transverse stress. For MF devices (Fig.1(a)) with $W_F\times N_F=2 \mu m \times 16, 1 \mu m \times 32,$ and $0.5 \mu m \times 64$, the smaller $W_F$ associated with larger $N_F$ will increase $\sigma_{//}$ and lead to lower $\mu_{eff}$ owing to the compressive $\sigma_{//}$ from STI [4]. As for the single-ring devices (Fig.1(b),(c)), the compressive $\sigma_{//}$ can be eliminated but $\sigma_{\perp}$ remains there, responsible for $\mu_{eff}$ degradation in n-MOSFETs. Thus, the single-ring layout with enlarged length of active region (LOD) is proposed to reduce $\sigma_{\perp}$. Herein, D1S1 (Fig.1(b)) denotes the typical rule, given by $LOD=0.36\mu m$ and $0.45\mu m$, corresponding to $S_{SDOD}=0.16\mu m$ and $S_{SDOD}=0.25\mu m$ at drain and source sides. D1S3 (Fig.1(c)) is specified with 3 time larger $S_{SDOD}$ to 0.75 $\mu m$, yielding LOD=0.95 $\mu m$ at the source sides. The enlarged LOD intends to effectively reduce $\sigma_{\perp}$ and recover $\mu_{eff}$. Taking the single-ring layout as the template, MR devices shown in Fig.2, with 4 rings and different LOD, namely W2N8R8_D1S1 and W2N4R8_D1S3 are designed, given with $W_F=2\mu m$, $R=4$, and $N_F=4\times R=16$. Also, MR devices with 8 rings can be implemented with $W_F=1\mu m$, $R=8$, and $N_F=4\times R=32$. Note that MF and MR devices follow the layout splits with fixed total width, $W_{tot}=W_F \times N_F=32\mu m$. Table 1 summarizes the basic device parameters extracted using our proprietary device parameters extraction method [5]-[6] in which $f_T$, $f_{MAX}$ or $C_{ox} (V_{gs})$ and $\Delta W$ are necessary for $\mu_{eff}$ extraction. Besides, the parasitic resistance $R_P$ is another key parameter to be known for an accurate $\mu_{eff}$ extraction from the measured I-V characteristics. Fig. 3 shows the $R_g$ determined by our transmission line (TLM) model [7] for MF and MR devices. The results indicate an approximately linear increase of $R_g$ versus $N_F$ and the MR devices can achieve around 16~30% smaller $R_g$ than MF devices with the same $W_F$ and $N_F$. The reduction of $R_g$ is an important factor besides the $\mu_{eff}$ enhancement for $g_m$ improvement.

III. Comparison of MR and MF Devices - $g_m$, $\mu_{eff}$, and $R_g$

In the following, a serious comparison between the MR and MF n-MOSFETs will be focused on three major device parameters, $g_m$, $\mu_{eff}$, and $R_g$ which are key factors responsible for the RF and analog performance, such as $f_T$, $f_{MAX}$, and RF noise. According to the analytical models expressed by (1)-(3) [8]-[9], $g_m$ is the most important parameter with direct and significant influence on $f_T$, $f_{MAX}$ and minimum noise figure ($NF_{min}$). Furthermore, $R_g$ has major impact on $f_{MAX}$, $NF_{min}$, and equivalent noise resistance ($R_n$) given by (2)-(4) [8].

$$f_T = \frac{g_m}{2\pi C_{gs}^2 - C_{gs}^2}$$

$$f_{MAX} = \frac{2\sqrt{R_g (g_m + 2\pi f_T C_{gs}) + g_m (R_g + R_s)}}{f_T}$$

$$F_{min} = 1 + \frac{f}{R_g} \sqrt{g_m (R_g + R_s)}$$

$$NF_{min} = 10\log (F_{min})$$

where, $C_{gs}$ and $C_{gd}$ represent the gate to drain capacitance, and total gate capacitance, which can be determined from the intrinsic $\gamma$-parameters after a dedicated open and short deembedding to the bottom metal layer, i.e. metal-1[8].

First, Fig. 4 (a) shows the $g_m$ versus $V_{GT}$ measured from the MF and MR n-MOSFETs in linear region ($V_{DS}=50$ mV). Note that $V_{GT}=(V_{DS}-V_{TH})$ is used to offset the $V_T$ variations between the devices with different layouts for a fair comparison. The results indicate that W1N32 with the smaller $W_F$ and larger $N_F$ in the MF layout suffers the lowest $g_m$ which reveals around 6% degradation compared to W2N16 and suggests the impact from STI $\sigma_{//}$ on $\mu_{eff}$ and longer source line on $R_g$. On the other hand, W2N4R4_D1S3 in the MR layout can offer the largest $g_m$, which is around 5% higher than W2N16 and 11% higher than W1N32. Then, taking MF devices as the reference, Fig. 4 (b) shows the increase of $g_m$ realized by MR devices compared with the reference with the same $W_F$ and $N_F$ and normalized to the reference, denoted as $\Delta g_m/g_m(MF)$. The results indicate that W1N4R8_D1S1 can yield...
5~7.2% higher $g_m$ than W1N32. However, the $\Delta g_m$/$g_m$(MF) achieved by W2N4R4_D1S1 w.r.t. W2N16 is below 3.6% and the $\Delta g_m$/$g_m$(MF) can be increased to around 6% by W2N4R4_D1S3 with enlarged LOD, attributed to reduced STI $\sigma_T$. Furthermore, the $\mu_{eff}$ can be extracted from the linear I-V model given by (5) in which the basic device parameters like $L_g$, $C_{ox(inv)}$, and $W_{eff}$ can be known from Table 1, determined by using our proprietary method [5]-[6] and the measured I$\text{DS}$(V$\text{GT}$, V$\text{DS}$). Fig. 5 (a) and (b) show the $\mu_{eff}$ versus V$\text{GT}$, extracted from the MF and MR n-MOSFETs with $W_f$=2µm and 1µm, respectively. The comparison of W2N4R4_D1S3 versus W2N16 and W1N4R8_D1S1 versus W1N32 indicates that the MR devices can achieve apparently higher $\mu_{eff}$ than the MF devices with the same $W_f$ and $N_F$. The results prove that the MR layout with eliminated STI $\sigma_T$ and reduced STI $\sigma_T$ from the enlarged LOD can contribute higher $\mu_{eff}$. Finally, Fig. 6 presents the $R_g$ determined by using Y-method, according to (6) [8]. The results indicate a significant $R_g$ reduction when increasing $N_F$ and around 10% lower $R_g$ in the MR devices than MF devices with the same $W_f$ and $N_F$. It means that the MR devices can simultaneously yield higher $g_m$ and lower $R_g$.

IV. Conclusion

The MR devices realized by 90nm CMOS process have been proven successful with significant $g_m$ enhancement over the MF devices, attributed to simultaneous improvement of $\mu_{eff}$ and $R_g$. Moreover, the MR devices can yield 10% smaller $R_g$. The higher $g_m$ and lower $R_g$ can contribute higher $f_T$ and $f_{MAX}$ as well as lower NF$\text{min}$ and $R_g$. These important features can facilitate RF and analog performance optimization.

Acknowledgement

This work is supported in part by the Ministry of Science and Technology under Grants MOST 104-2221-E-009-116-MY3. Besides, the authors acknowledge the support from CIC for test chip fabrication and NDL for devices measurement.

References