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A Gain Cell Array with Retention Increment Design for Bit-Area Efficient On-Chip Memory Applications

Sivasundar Manisankar, Hyunmyoung Kim and Yeonbae Chung

School of Electronics Engineering, Kyungpook National University
80 Daehak-Ro, Book-Gu, Daegu, 41566, Rep. of Korea
Phone: +82-53-950-5522, E-mail: ybchung@ee.knu.ac.kr

Abstract

This work presents a novel circuit design to improve the data retention of logic-compatible gain cell DRAM. The proposed design utilizes a parasitic capacitance built between the common cell-body and the data storage node. During data write, a voltage toggle on the cell-body couples down the data storage levels. It results in enhancing the data retention in a compact bit-area. The technique also provides much strong immunity from the write disturbance. Measured results at 1.2 V and 85 ℃ from a 110 nm 64-kbit eDRAM test chip exhibit 63.6 % improved retention time over the conventional design.

1. Introduction

Logic-compatible gain cell DRAMs are drawing a growing attention due to their favorable embedded attributes [1–5]. Featuring compact bit-area, dual-port functionality, decoupled read-write path and non-destructive read-out, the gain cell DRAMs are becoming a promising alternative to SRAMs which have been the mainstream embedded memory of choice. Attaining practical retention time along with competitive bit-density over SRAMs remains as a major challenge. In this work, we explore a dual threshold voltage (V_{TH}) two-transistor (2T) gain cell DRAM with a novel write-back technique. This technique enhances the data retention and the write disturbance immunity without using additional cell devices. All the results in this work were obtained in a 110 nm logic CMOS technology.

2. Gain Cell DRAM with Body-Toggled Write-Back

Fig. 1 shows the PMOS-based 2T gain cell schematic, layout and its device cross-sectional view implemented in logic CMOS technology. The memory cell consists of a high-V_{TH} write transistor and a standard-V_{TH} read transistor. The circuit technique in this work utilizes the parasitic capacitance (C_{JP}) of a reverse-biased p-n junction formed between the n-well and the cell data-node (DN) by toggling the common cell-body (BD_C) rather than connecting to V_{DD}, thereby improving the data retention.

Fig. 2 shows a simplified memory array circuits, and Fig. 3 illustrates the bit-cell bias conditions and capacitive couplings on DN for each operating mode. During the standby, both the read-bitline (RBL) and the write-bitline (WBL) are sustained to the ground. The write-wordline (WWL) and the read-wordline (RWL) are set to V_{DD} and the ground, respectively. BD_C is tied to V_{DD}. For the read operation, RWL is pulled up to V_{DD} after the bitline (BL) precharge transistors are disabled. This RWL transition couples up the DN voltages through the gate-to-RWL overlap capacitance of the

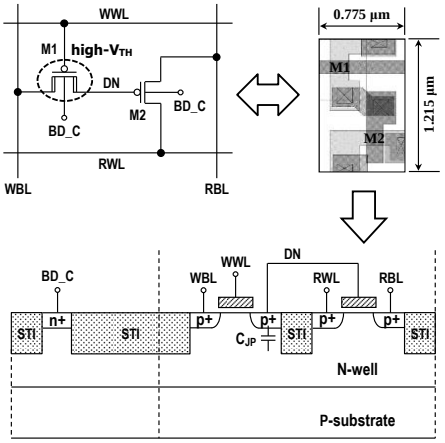

Fig. 1 2T gain cell schematic, layout and its device cross-sectional view.

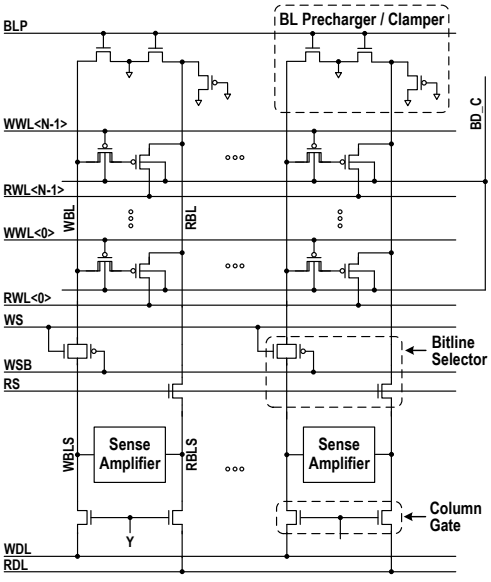

Fig. 2 Simplified memory array circuits.

read transistor. The read path either turns on or stays off depending on the DN status. If DN is high, the read-PMOS does not turn on so that RBL will be maintained to the ground. If DN is low, the read-PMOS turns on and thus a cell charging current will flow from RWL to RBL. This raises the voltage level of RBL which is self-clamped once it rises above V_{TH} of PMOS. This read signal is forwarded to RBLS by switching RS high. Before sensing the data, RS is set to low again to prevent the full-swing voltage being

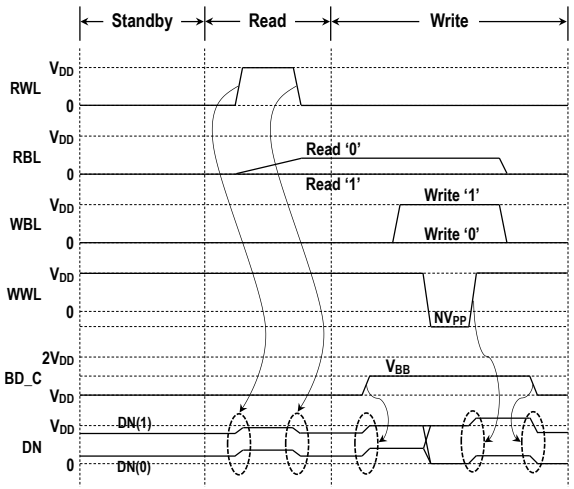

Fig. 3 Bit-cell bias conditions and capacitive couplings on DN for each operating mode.

propagated back to RBL. Then, the sense amplifier (SA) samples the data states.

For the write operation, the external data for the selected column are developed on SA bitlines (WBLS, RBLS) when the column decoding signal Y is enabled. Then, the common BD_C is set to a boosted voltage V_{BB}. This couples up both initially stored data '1' and '0' voltages through the parasitic coupling device (C_{JP}). In this design, V_{BB} is $1.35V_{DD}$. Next, WS and WSB are triggered to connect WBL and WBLS together. Afterward, WWL is set to a negative voltage NV_{PP} allowing a new data to be written into the cell. Because of a boosted voltage on BD_C, this injects less charge into DN compared to the one operating with BD_C kept to V_{DD}. Next, WWL is pulled up to V_{DD}. The WWL transition also couples up both data '1' and '0' voltages through the gate-to-DN overlap capacitance of the write transistor. Then, BD_C is finally switched back to V_{DD}. This couples down both data '1' and '0' storage voltages, fully restoring the cell data '0' storage level. The lower data '0' level increases the cell data retention time. It also drives a large read cell-current for the read transistor, enhancing the read performance. The slightly lowered data '1' level does not affect the data retention since the data '1' destruction is self-protected better than the data '0' loss in all-PMOS cells [2]. Another benefit of the proposed write-back technique is to increase the write '1' disturbance immunity in the nature. Especially when data '1' is written to a bit-cell, the data '0' levels stored in unselected cells on the same WBL are destroyed by the subthreshold leakage through the write devices. This disturbance may be vital to data retention. In the proposed technique, the subthreshold leakage in unselected cells is drastically reduced owing to a negative source-to-body voltage on the write transistors.

The proposed technique has been designed and fabricated in a 64-kbit eDRAM. The memory contains a test circuit to monitor the chip features according to with or without cell-body toggle. The chip photograph and the data I/O waveforms measured at 1.2 V room temperature are shown in Fig. 4. The cycle begins on the rising edge of the clock (CLK). The input data '10100110' are written in series into

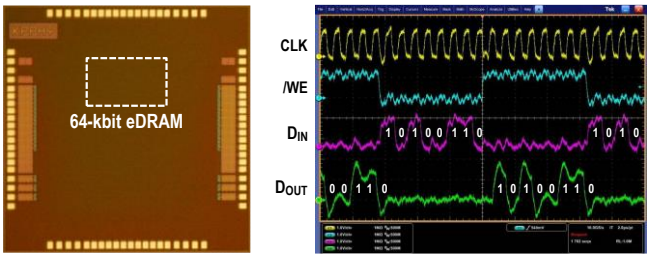

Fig. 4 Chip photograph and measured data I/O waveforms.

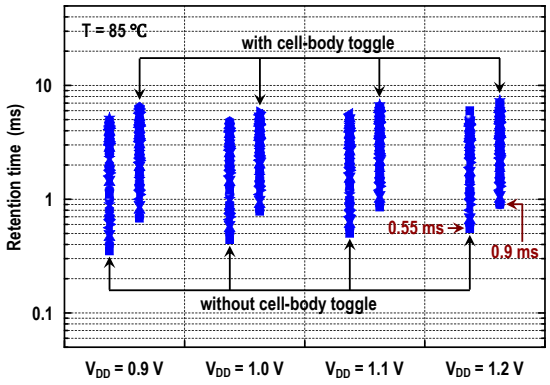

Fig. 5 Retention time distribution measured at T = 85 ℃.

the chip when /WE is low. Then, the output data are read in series with the same address sequence when the /WE is high. The output data match the input completely. Fig. 5 displays the retention time distribution including cell-to-cell variation. The retention time at 85 ℃ has been measured by detecting failure bits over the 64-kbit cell array running at a minimum cycle. For the eDRAM operating at 1.2 V with cell-body toggle, a cumulative average retention time is 2.86 ms with a minimum of 0.9 ms, while a cumulative average is 2.02 ms with a minimum of 0.55 ms for the eDRAM operating at the same supply voltage without cell-body toggle. The minimum retention time is improved by 63.6 %.

3. Conclusion

We described a logic 2T DRAM with cell-body toggled write-back scheme. Measurement results from a 64-kbit test chip fabricated in 110 nm logic process exhibit much improved data retention. The proposed technique in this work can be applicable to the more scaled CMOS technology.

Acknowledgment

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References

[1] D. Somasekhar *et al*., IEEE J. Solid-State Circuits **44** (2009) 174.
[2] K. C. Chun *et al*., IEEE J. Solid-State Circuits **46** (2011) 1495.
[3] K. C. Chun *et al*., IEEE J. Solid-State Circuits **47** (2012) 2517.
[4] W. Cheng *et al*., IET Circuits Devices Syst. **8** (2014) 107.
[5] W. Choi *et al*., IEEE J. Solid-State Circuits **50** (2015) 2451.