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An All-Digital Duty-Cycle Corrector with Synchronous and High Accuracy Output for DDR-SDRAM Application

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Abstract

A synchronous and high accuracy all-digital duty-cycle corrector (ADDCC) is presented in this paper. The proposed ADDCC utilizes simplified dual-loop architecture for synchronous and high accuracy output. The measurement results show proposed ADDCC can operate from 300 MHz to 600 MHz with input duty-cycle range 40~60%, and the output duty-cycle error is less than 1% with a RMS jitter of 3.86 ps.

1. Introduction

In modern high-speed circuits and systems, a clock with accurate 50% duty-cycle is very important. These applications, such as double data rate (DDR) memory and SDRAM, utilize both rising and falling edge of clock to double data rate. Therefore, a duty-cycle corrector (DCC) is required to ensure 50% duty-cycle clock [1]-[4]. In this paper, a feedback all-digital duty-cycle corrector (ADDCC) with synchronous and high accuracy output is presented. The proposed ADDCC utilizes simplified dual-loop architecture to achieve a synchronous and accurate 50% duty-cycle output.

2. Proposed All-Digital Duty-Cycle Corrector

The proposed ADDCC exploits a simplified dual-loop architecture, namely control loop and delay loop, as shown in Fig. 1. To explain the operation principle, a timing diagram of proposed ADDCC is shown in Fig. 2. Initially, signal Q_clk is set to high by signal Ini_clk. When input clock Ref_clk is activated, the rising edge triggers D flip-flop (DFF) to change signal Q_clk from high to low. According to the control code F[6:0], the digital-controlled delay line (DCDL) generates a varied delay clock Out_clk from Q_clk and triggers the pulse generator (PG). After that, the PG outputs a narrow pulse and sets signal Q_clk and Out_clk back to high. Until now, the delay loop completes first period of Out_clk and waits for Ref_clk input again. In the control loop, the phase detector (PD) outputs signal Up and Dn by compares phase of signal Ref_clk and Out_clk. After that, the control circuit (CC) converts pulse signal Up and Dn to up/dn counter control signal Upc and Dnc and adjust the delay of DCDL by 7-bit control code F[6:0]. After several cycle, the output signal Out_clk is synchronous with input clock Ref_clk. Meanwhile, the output period is just twice of delay of DCDL, ensure a 50% duty-cycle output. Therefore, due to simplified dual-loop architecture, a synchronous and high accuracy 50% duty-cycle output is provided.

3. Experimental Results

The proposed ADDCC has been fabricated in a 0.18-μm CMOS process with a 1.8-V supply voltage. Fig. 3 shows the die photo of proposed ADDCC; the active area is only 0.091 mm^2. As shown in Fig. 4 and Fig. 5, the output duty-cycle at 600 MHz input clock with 40% and 60% duty-cycle is 50.19% and 50.15%, respectively. And the static phase error is 26.93 ps and 18.84 ps, respectively. Additionally, the peak-to-peak jitter is 28.75 ps and RMS jitter is 3.86 ps while 600 MHz input frequency and 60% input duty-cycle, as shown in Fig. 6. The variation of output duty-cycle is less than 1% when varied input frequency and duty-cycle, as shown in Fig. 7. For convenience, Table I summarizes current state-of-art all-digital DCCs [3], [4].

4. Conclusions

A synchronous and high accuracy all-digital duty-cycle corrector is presented. Due to the simplified dual-loop architecture, a synchronous output is generated and duty-cycle error is less than 1% with varied input clock frequency and duty-cycle. Therefore, the proposed ADDCC is suitable for applications such as DDR memory and SDRAM.

References

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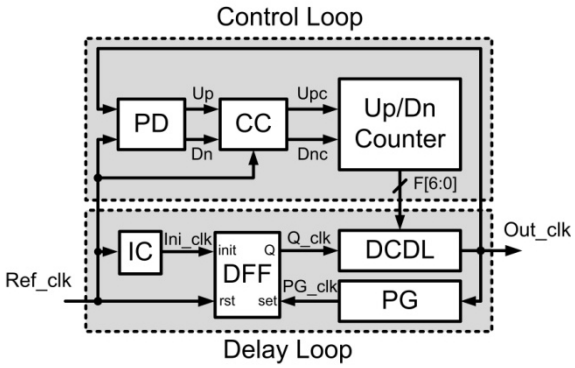

Fig. 1. Proposed all-digital synchronous duty-cycle corrector.

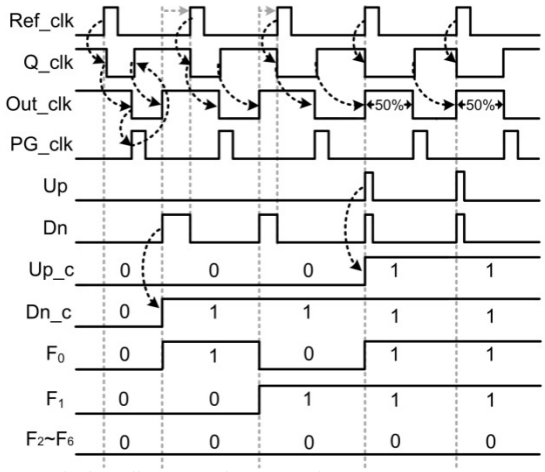

Fig. 2. Timing diagram of proposed ADDCC.

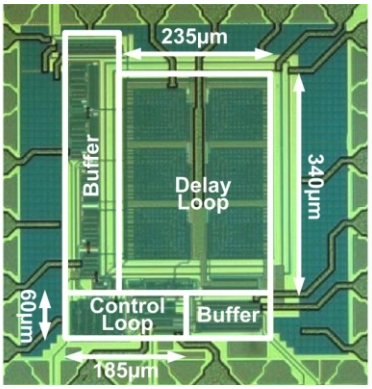

Fig. 3. The die photo of proposed ADDCC.

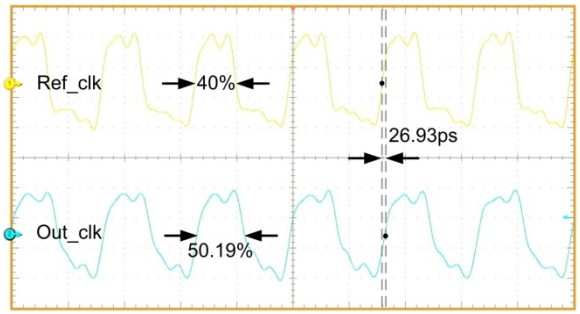

Fig. 4. Measurement waveform with input clock of 600 MHz and 40% input duty-cycle.

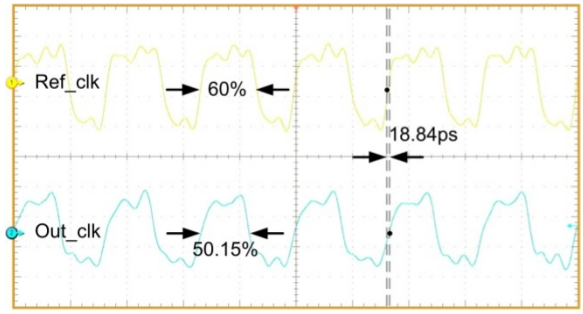

Fig. 5. Measurement waveform with input clock of 600 MHz and 60% input duty-cycle.

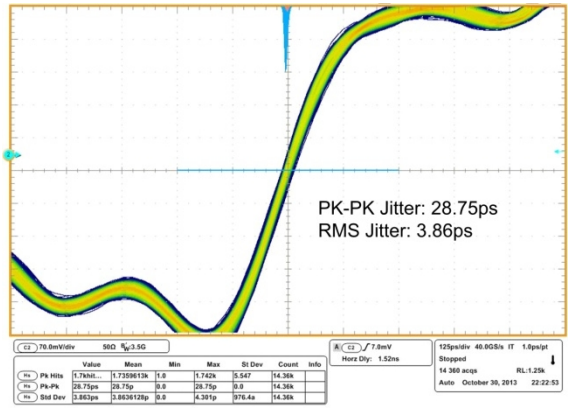

Fig. 6. Jitter histogram of corrected output at 600 MHz and 60% input duty-cycle.

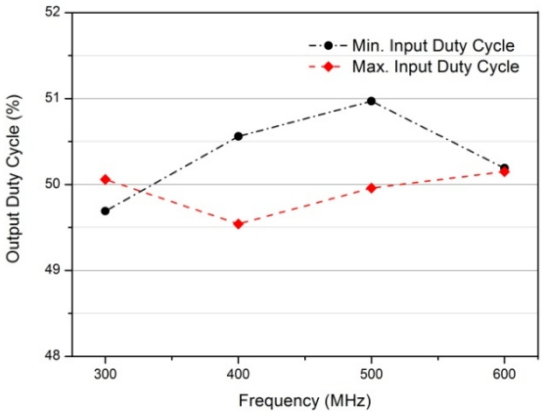

Fig. 7. Output duty-cycle range.

TABLE I. PERFORMANCE COMPARISON OF ALL-DIGITAL DCCS

	[3]	[4]	This Work
Technology	0.18 μm	0.18 μm	0.18 μm
Frequency Range	800 MHz ~ 1.2 GHz	250 MHz ~ 625 MHz	300 MHz ~ 600 MHz
Correction Range	40% ~ 60 %	30% ~ 70%	40% ~ 60%
Duty-Cycle Error	–1.4% ~ 1.5%	< 1.6%	–0.5% ~ 1%
$Jitter_{p2p}$ (ps)	12.9 (1.29%) @ 1 GHz	21.1 (1.74%) @ 625 MHz	28.75 (1.72%) @ 600 MHz
$Jitter_{rms}$ (ps)	N / A	2.79 (0.17%) @ 625 MHz	3.86 (0.23%) @ 600 MHz
Power	15 mW	10.8 mW @ 625 MHz	18 mW @ 600 MHz