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Perspective Analysis of tri-Gate Germanium Tunneling Field Effect Transistor with Dopant Segregation Region at Source/Drain

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ABSTRACT

Numerical simulation of *n*-channel tri-gate germanium Tunneling Field Effect Transistor (TFET) with dopant segregated region at source/drain (DS-TFET) is conducted with TCAD tools. The characteristics of the devices are compared and analyzed. It's found that tri-gate DS-TFET's performance is insensitive to dopant concentration and barrier height of *n*-type drain, while dopant concentration and barrier height of *p*-type source have considerable impact on that with positive bias state on the device. It is considered to be attributed to domination of electron current in the whole BTBT current.

1. INTRODUCTION

Up to now, silicon has faced tremendous challenges on scaling down of MOSFET devices [1]. Because of higher mobility, germanium has been widely studied and seen as a candidate for the replacement of silicon material. Meanwhile, for many low power applications, Tunneling-Field-Effect transistor (TFET) owns instinctive superiority over traditional MOSFET due to its tunneling mechanism without 60mV/dec limit on Subthreshold Swing (*SS*) [2-4]. Previously Schottky type TFET (S-TFET) based on silicon has been investigated [5]. It inherits the advantages of TFET with steep *SS*, and superior to conventional TFET with less complexity of manufacture process and lower thermal budget, but still suffering from relatively low ON-state current. In this work, we discuss on the application of germanium material as the device channel, and dopant segregation source/drain for TFET (DS-TFET), in order to weaken the effect of barrier height and improve its performance.

2. DEVICE STRUCTURE AND SIMULATION PARAMETERS

Schematic device structure of DS-TFET is presented in *Fig*.1. Tri-gate is applied as the default and dual-gate is also simulated for comparison. Channel length is set to be 16nm for both tri-gate, and dual-gate cases. Equivalent gate oxide thickness is equal to 1nm (assuming HfO_2 as gate dielectric material). In *Fig*.1, the width and thickness of the channel are the same as 20nm (L_w) to get a square cross-section. The length of segregation region at source/drain (L_{sd}) makes 10nm and doping concentration for both segregation regions takes $10^{19}cm^{-3}$ as default, with boron and phosphorus as dopant respectively. Intrinsic germanium channel is applied. To investigate the impact of Schottky contacts combining with the dopant segregation, both barrier heights (SBH/s for source and SBH/d for drain) are assigned ranging from 0.2 to 0.6eV respectively. Besides, device operating temperature has been varied from 250 to 350K. Synopsys Sentaurus TCAD tool is used as simulation platform. All simulations apply V_{dd}=0.5V if not mentioned. Band to Band tunneling model is added for all kinds of simulation. Wentzel-Kramers-Brilliouin (WKB) model is applied for calculating the current through the Schottky contacts. Furthermore, Trap Assistant Tunneling (TAT) model is newly added and trap concentrations on source and drain are set to $10^{12}cm^{-3}$ [6]. Regular models such as Hydrodynamic model, Fermi distribution are also included in this work.

3. RESULTS AND DISCUSSIONS

As shown in *Fig*.2(a), a batch of similar transfer curves are illustrated with various SBH/d and fixed SBH/s. Dopant concentration and L_{sd} are using the default value. Only a small difference is observed near zero gate voltage. For comparison, *in vice versa*, we fix SBH/d and change SBH/s value, the simulated results are shown in *Fig*.2(b). Interestingly, the transfer curves begin to separate at a large degree following with increasing drain current as the barrier height gets higher. It is expected that the higher SBH, no matter for source or drain side, will deteriorate the performance of MOSFET. However, for DS-TFET, its current composition mainly comes from BTBT tunneling current more concisely, and the BTBT electron current under positive gate bias is dominated by SBH/s. As shown in *Fig*.3, SBH/d only affects hole current instead of electron current, so in view of total current curves, SBH/d has a much smaller impact to the whole curve.

Due to the same reason, diversion happens for the simulation of performance with various boron dopant concentration and phosphorus dopant concentration, as shown in *Fig*.4. It is found that dopant concentration at drain-side has little effect on the total current density. As contrast, source-side dopant concentration changes the curve radically with a heavier doping current increases or it could be equivalent to lower barrier height at source. And barrier height's influence on I_{on} and I_{min} (minimum current value on *I-V* curve) has been illustrated in *Fig*.5. *Fig*.6-7 shows the effect of L_{sd}. With longer L_{sd}, I_{on} and I_{min} move downside at the same time, because of the higher source/drain resistance. *Fig*.8 displays *SS* characteristic under different SBHs and temperatures. SBH/s keeps the biggest impact factor: *SS* rises fast as SBH/s increases while temperature contributes a relatively small influence. But even with barrier height of 0.6eV, DS-TFET retains low *SS* (lower than 80mV/dec).

Fig.9 shows the transfer curves of dual-gate DS-TFET and tri-gate DS-TFET under different temperature. Tri-gate DS-TFET has a nearly 35% enhancement in ON-state current than dual-gate DS-TFET does under all tested temperatures. And it shows clearly a distinct difference in distribution of electrostatic potential from *Fig*.10-11. Tri-gate DS-TFET's electrostatic potential and current distribution shape as an arch surrounded by the gate. Regular parallel line is a typical distribution of dual-gate structure where the electric field is symmetric.

4. Conclusions

We did comprehensive investigation on tri-gate germanium based DS-TFET. Asymmetric reaction to dopant concentration and barrier height of source and drain has been found and explained which could be utilized relieving the am-bipolar effect and strict manufacture requirements. Tri-gate DS-TFET has a better performance than dual-gate DS-TFET. Additionally, with

a high I_{on}/I_{off} and extremely low *SS*, tri-gate germanium DS-TFET is promising for ultra-low power applications.

Acknowledgement

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References

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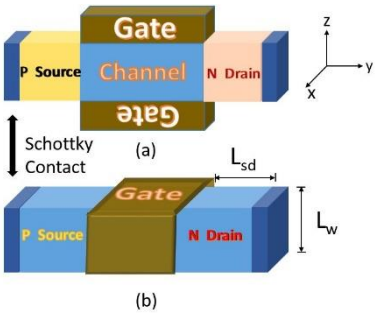

*Fig.*1 Device structure diagram of (*a*) dual-Gate TFET. (*b*) tri-Gate TFET (both on Germanium).

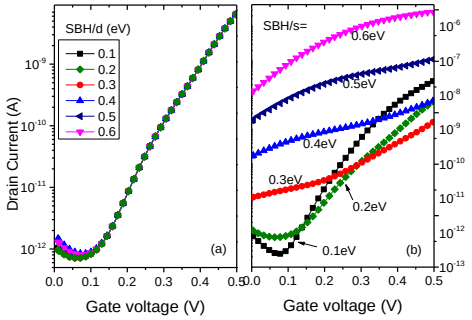

*Fig.*2 Transfer characteristics of tri-Gate TFET (*a*) SBH/s=0.2eV with different SBH/d in step of 0.1eV. (*b*) SBH/d=0.2eV with different SBH/s in step of 0. 1eV, both from 0.1 to 0.6 eV.

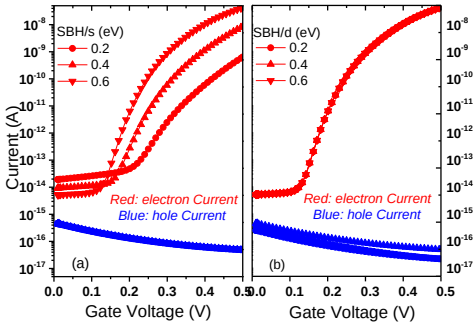

*Fig.*3 Electron and hole current under various SBHs (*a*) at fixed SBH/d=0.2eV. (*b*) at fixed SBH/s=0.2eV.

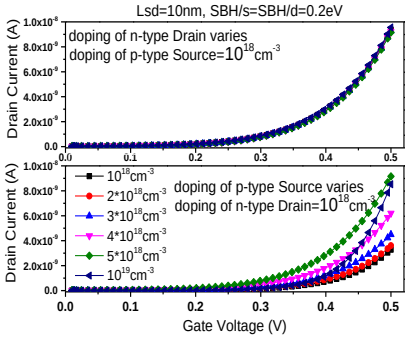

*Fig.*4 Transfer curves of tri-Gate TFET. SBH/d=0.2eV and SBH/s=0.2eV with different phosphorus (upper) and boron (lower) doping concentration from 10^{18} cm^{-3} to 10^{19} cm^{-3}.

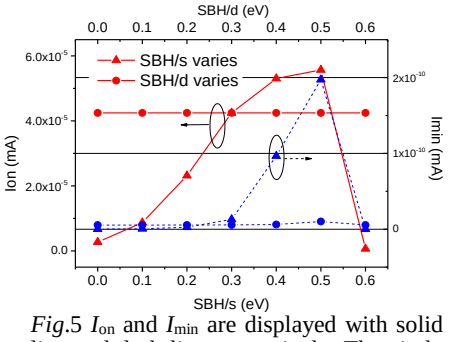

*Fig.*5 I_{on} and I_{min} are displayed with solid line and dash line respectively. The circle represents SBH/s = 0.2eV while SBH/d varies and triangle represents fixed SBH/d = 0.2eV when SBH/s varies.

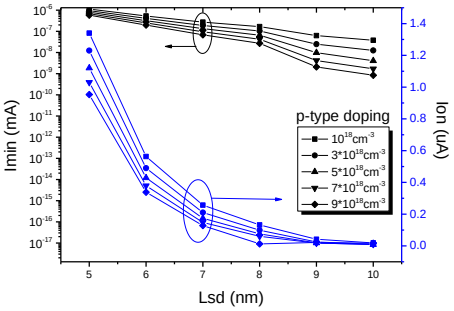

*Fig.*6 I_{on} and I_{min} based on different L_{sd} while the *p*-type dopant concentration varies from 10^{18} cm^{-3} to 9x10^{18} cm^{-3} where *n*-type dopant concentration fixed at 10^{19} cm^{-3} and barriers are both set 0.2eV.

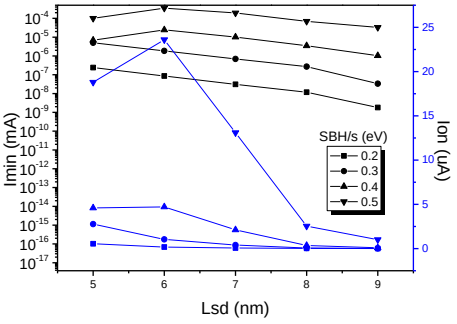

*Fig.*7 I_{on} and I_{min} based on different L_{sd} while the SBH/s varies from 0.2eV to 0.5 eV where *n*-type and *p*-type dopant concentration fixed at 10^{18} cm^{-3} and 10^{19} cm^{-3} respectively.

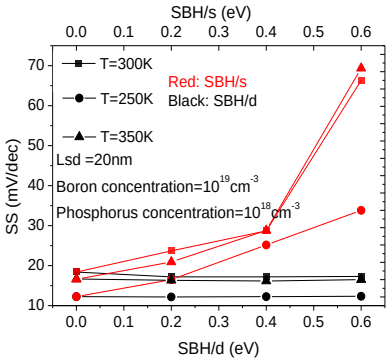

*Fig.*8 Subthrehold Swing of tri-gate TFET with different SBH/s, SBH/d and temperature.

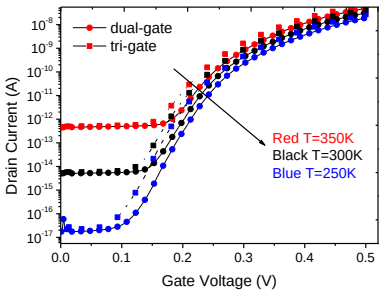

*Fig.*9 Transfer curves of dual-gate and tri-gate DS-TFETs under 250, 300, 350K with L_{sd}=20nm, *n*/*p* doping equals 10^{18} and 10^{19}cm^{-3} respectively.

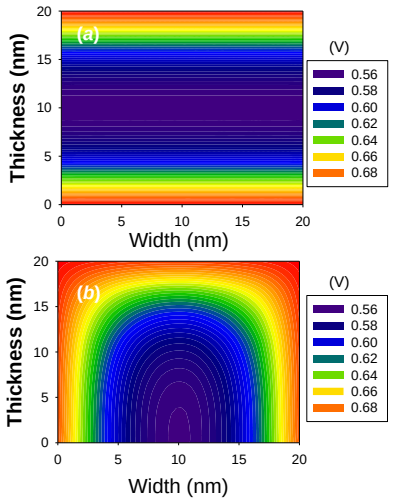

*Fig.*10 ON-state electrotatic potential distributions of (a) dual-Gate TFET. (b) tri-Gate TFET (Cross-section perpendicular to Y-direction)

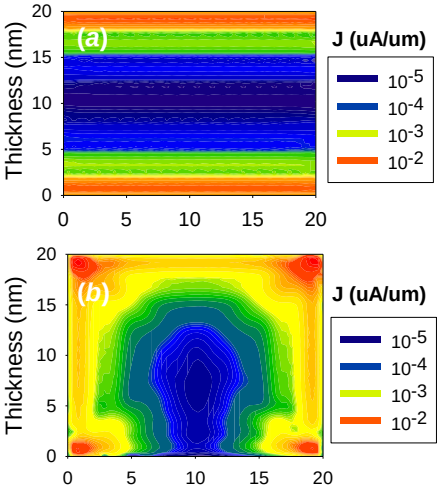

*Fig.*11 Current distributions of (*a*) dual-Gate DS-TFET. (*b*) tri-Gate DS-TFET (Cross-section perpendicular to Y-direction)