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Influence of Line-Edge Roughness (LER) on Multiple-Gate (MG) Tunnel Field-Effect Transistors (TFETs)

Woo Young Choi, Song Hun Choi, Jang Woo Lee, and In Huh

Department of Electronic Engineering, Sogang University
35 Baekbeom-ro (Sinsu-dong), Mapo-gu, Seoul 04107, Republic of Korea

Abstract

The influence of fin- and gate-line-edge roughness (LER) on multiple-gate (MG) tunnel field-effect transistors (TFETs) has been investigated compared with metal-oxide-semiconductor FETs (MOSFETs) by using full three-dimensional simulation. Two interesting results have been observed. First, MG TFETs show ignorable gate-LER unlike MG MOSFETs, which means that only fin-LER can be considered when evaluating the total LER of MG TFETs. Second, TFETs show ~3x more LER improvement than MOSFETs when their structures are changed from double-gate (DG) to triple-gate (TG) types. Our findings provide useful design guidelines of variation-tolerant TFETs.

1. Introduction

A tunnel field-effect transistor (TFET) has been regarded as one of the most promising abrupt switching electron devices thanks to good complementary metal-oxide-semiconductor (CMOS) process compatibility [1]. On the other hand, it means that a TFET may suffer from the same performance variation sources as a MOSFET [2]. This manuscript contributes to the line-edge roughness (LER) [2,3,4,5] of fin-type multiple-gate (MG) TFETs including double-gate (DG) and tri-gate (TG) structures. It was previously reported that fin-LER was a dominant variation source of DG TFETs based on two-dimensional simulation [6]. Unlike the previous work, this manuscript focuses on the following two issues. First, the influence of gate- and fin-LER on MG TFETs will be compared comprehensively by using full three-dimensional device simulation. Second, the advantages of TG TFETs over DG ones will be confirmed in terms of gate- and fin-LER.

Fig. 1 shows the schematics of the simulated devices. Only n-channel MOSFETs and TFETs will be discussed for simplicity. Three-dimensional device simulation has been performed by using commercial simulators [7]. Simulated parameters are listed in Table 1. 200 device structures of MG TFETs and MOSFETs have been generated, respectively.

2. Simulation results and discussion

Fig. 2 shows the simulated transfer curves of MG MOSFETs and TFETs under the influence of fin- and gate-LER. Fig. 3 summarizes the σV_{th} and σSS values of each case. From Figs. 2 and 3, two noteworthy things have been observed. First, gate-LER is less significant in the case of MG TFETs than in the case of MG MOSFETs. It is because the electrical characteristics of TFETs are determined around the narrow source-to-channel tunnel junction region rather than the entire channel. Thus, the total LER of MG TFETs can be evaluated only by considering fin-LER. In order to confirm the idea, the potential distributions of the highest and lowest V_{th} cases under the influence of fin- and gate-LER are shown in Fig. 4. The potential distributions of nominal devices are also shown for comparison. Figs. 4a and c show that fin-LER affects both MG TFETs and MOSFETs significantly. In the case of the former, considerable tunneling barrier width fluctuation occurs due to fin-LER. Also, in the case of the latter, source-to-channel energy barrier height fluctuates as a function of fin-LER. On the contrary, Figs. 4b and d show that gate-LER affects MG MOSFETs more than MG TFETs. In the case of the latter, the lateral electric field penetration from the drain is fluctuated by gate-LER, which leads to the source-to-channel energy barrier height comparable with fin-LER. However, in case of the former, the tunneling barrier width fluctuation is ignorable because the potential near the source-to-channel junction is rarely varied by gate-LER.

Second, MG TFETs show ~3x more LER reduction in terms of σV_{th} and σSS than MG MOSFETs when device structures are changed from DG into TG. It is originated from their structure differences. MOSFETs have two n-p source-to-channel and drain-to-channel junctions. From the fin surface toward fin bulk, the gate controllability weakens. Thus, both source and drain potentials easily penetrate into the fin bulk. In the sub-threshold regime, MOSFETs have higher channel potential at the fin bulk than at the fin surface. It means that the sub-threshold characteristics of MG MOSFETs including V_{th} and SS are determined at the fin bulk rather than at the fin surface. It is because the fin bulk whose channel potential is higher than the fin surface provides sub-threshold current path.

3. Summary

The influence of fin- and gate-LER on MG TFETs has been discussed in comparison with MG MOSFETs. Two interesting facts have been revealed based on their operation principle differences. First, the total LER of MG TFETs can be estimated only by fin-LER because they have much weaker gate-LER than fin-LER. Second, in order to suppress total LER, the transition from DG to TG structures is more desirable for TFETs than for MOSFETs. This work will contribute to the design of variation-tolerant TFETs.

Acknowledgements

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Baravelli E, Jurczak, Speciale N, De Meyer K and Dixit A 2008 *IEEE Trans. Nanotechnol* **7** 291-8. [6] Baravelli E, Dixit A, Rooyackers R, Jurczak M, Speciale N and De Meyer K 2007 *IEEE Trans. Electron Devices* **54** 2466-74. [7] Sentaurus Device User Guide Version: H-2013.03, Synopsys, 2013

TABLE I. REFERENCE DEVICE PARAMETERS

	TFETS		MOSFETS	
Structure	DG	TG	DG	TG
Gate length (L_g)	20 nm			
Fin width (W_{fin})	7 nm			
Fin height (H_{fin})	15 nm	11.5 nm	15 nm	11.5 nm
Gate work function	4.08 eV	4.10 eV	4.80 eV	4.78 eV
Top-gate oxide thickness ($t_{ox,top}$)	30 nm	0.5 nm	30 nm	0.5 nm
Supply voltage (V_{DD})	0.9 V			

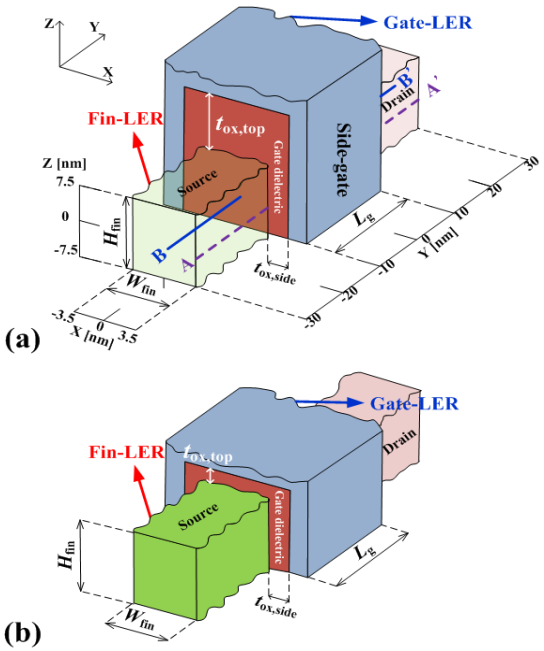

Fig. 1. Schematics of a (a) DG and (b) TG structure under the influence of gate- and fin-LER.

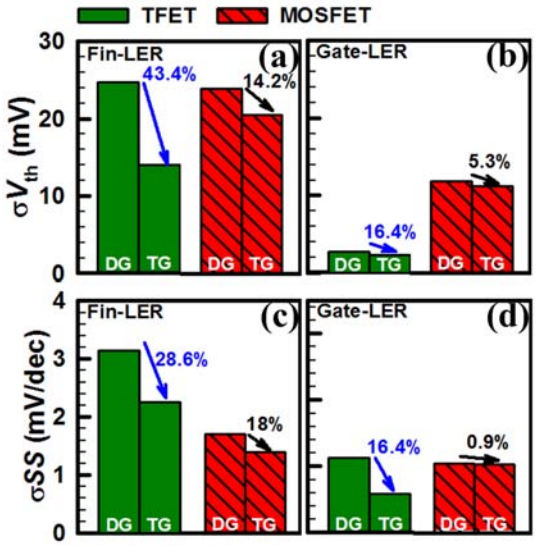

Fig. 3. σV_{th} due to (a) fin-LER and (b) gate-LER. σSS due to (c) fin-LER and (d) gate-LER.

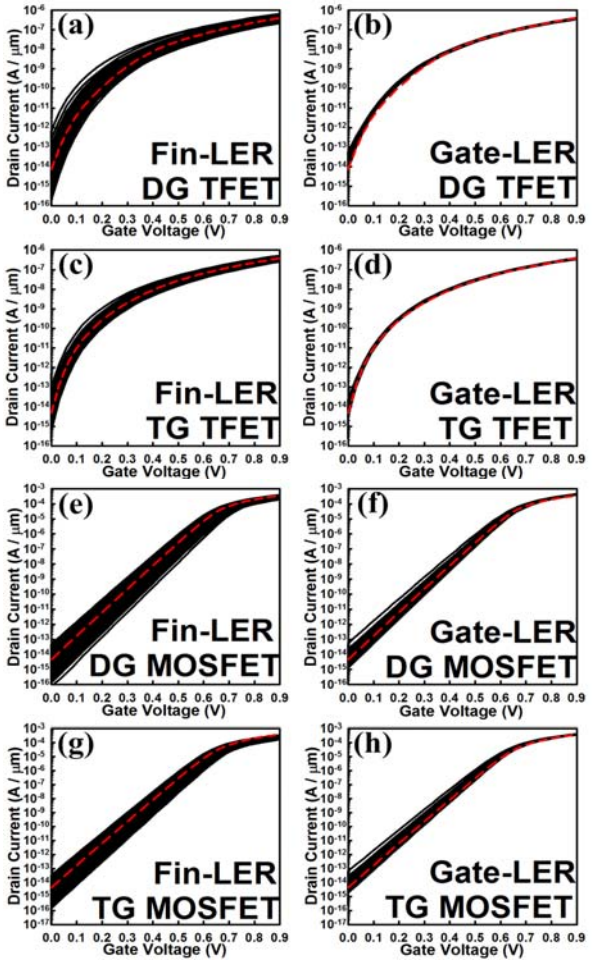

Fig. 2. Transfer curves of 200 generated MG TFETs and MOSFETs. Red lines correspond to the transfer curves of nominal devices.

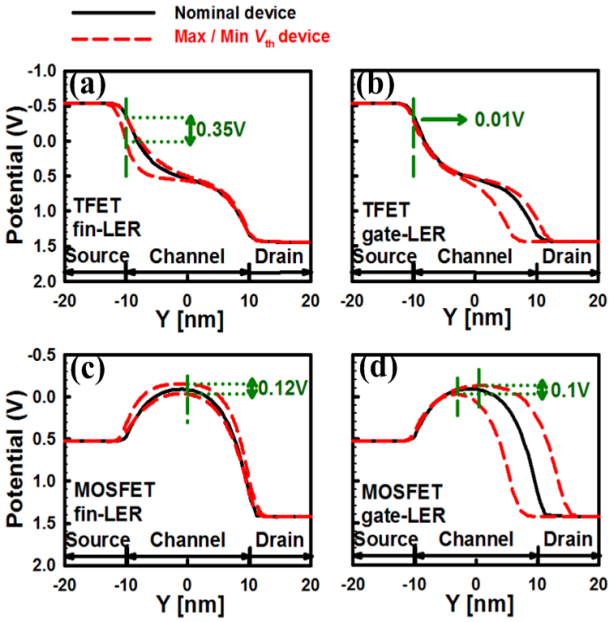

Fig. 4. Off-state potential distributions of DG TFETs under (a) fin-LER and (b) gate-LER and DG MOSFETs under (c) fin-LER and (d) gate-LER. Potentials have been extracted along the B-B' lines shown in Fig. 1. Dashed red lines represent the highest and lowest V_{th} cases and black solid lines represent the nominal case.