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Study of Self-heating Effects in Hybrid SOI/bulk Nanoscale FinFETs

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Abstract

Self-heating in SOI FinFETs is a major concern despite its advantages as compared to bulk FinFETs. Hybrid FinFETs are shown to have advantages of both bulk and SOI FinFETs. In this paper, we show that hybrid FinFETs show less self-heating and on-current degradation as compared to SOI FinFETs through 3-D electro thermal simulations. Different hybrid combinations are considered and their thermal effects are studied for various substrate and interconnect heights. We demonstrate that hybrid FinFETs can achieve similar thermal characteristics as that of bulk FinFETs for small substrate thickness.

1. Introduction

Self-heating is one of the important design considerations of nanoscale FinFET design. Low thermal conductivity of the thin silicon films and thermally insulating SiO_2 in FinFETs cause increased heating with large power input [1]. Self-heating effects in bulk FinFETs is less as compared to SOI FinFETs [2]-[3]. Though the fabrication of SOI FinFET is easier, contacting the body node is structurally challenging for thicker fins, which is essential for matching in circuits [4]. Fin width and fin height variability in bulk FinFETs is large (~150% more than that of SOI FinFETs) and doping the lower fin region is difficult. The cost difference between SOI FinFET and bulk FinFET is less than 3.4% for high volume fabrication [5]. A hybrid FinFET with bulk and SOI integration will have the advantageous of both SOI FinFET and bulk FinFET. The possible fabrication of such a device is discussed in [4]. Such devices will have less variability, better performance and reduced self-heating. Substrate thickness and interconnect structure are the two important parameters which determines the extent of heating in FinFET devices [2], [3], [6].

2. Self-heating Simulation in Hybrid FinFETs

Calibration

3D Electro-thermal TCAD tool based simulations have been used for the study of self-heating in hybrid FinFETs and for their comparisons with SOI and bulk FinFETs. Detailed TCAD model dc and thermal calibration with 14nm technology is explained in our previous work [3]. Mobility degradation, stress values, S/D distribution resistance and the gate work function are tuned to match the simulation results with the experimental data [7]. Thickness dependent thermal conductivity, thermal modeling of realistic back-end-of the line interconnect structure and interface thermal resistances are modeled for the thermal simulation. Thermal simulations are matched with the experimental data [8] to validate our thermal modeling [3].

The 3-D device structures used for simulation of five fin 14nm hybrid FinFETs (SBSBS and SBBBS) are shown in Fig. 1. Five different fin combinations of FinFETs are realized for comparisons (SOI FinFET (SSSSS), bulk FinFET (BBBBB) and three hybrid combinations). Table 2 lists the performance characteristics of different combinations. On-current decreases from SOI FinFET to bulk FinFET for the same I_{off} condition and the body effect increases. Fig. 2 shows the top view of the temperature distribution in four different configurations. We have observed that the introduction of bulk fin structure in between SOI fin structure reduces the self-heating in hybrid devices (The power input to each fin is kept the same to have a better comparison). Fig. 3 shows the side view of the temperature distribution in fins. Figure clearly shows the reduction in temperature in the fins with the introduction of bulk fin structure. The lower fin in the bulk fin structure helps in spreading the heat generated in the upper fins to reduce the heating. Fig. 4 illustrates the lattice temperature on top of the fins where the maximum heating occurs. In hybrid structures average temperature in the fins is less as compared to SOI FinFETs.

We have also compared the maximum lattice temperature and thermal resistance (R_{th}) of the devices with different interconnect heights and substrate thicknesses. Temperature increases with increase in interconnect heights, and heating in hybrid FinFETs is in between SOI and bulk FinFETs (Fig. 5). We have observed a significant improvement in the thermal resistance and the maximum lattice temperature of hybrid FinFETs for small substrate thicknesses. Self-heating dependent current degradation is shown in Fig. 6. Results show that % current degradation is less for hybrid FinFETs as compared to SOI FinFETs. This further decreases with reduction in substrate thickness.

3. Conclusions

We show through 3D electro-thermal simulations that hybrid FinFETs perform much better than SOI FinFETs in self-heating effects. Hybrid FinFETs have less thermal resistance and on-current degradation as compared to SOI FinFETs. Hybrid FinFETs show a similar thermal performance as that of bulk FinFETs for small substrate thickness.

References

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Table 1: FinFET Device Parameters

Channel length (L_g)	20nm
Fin Width (T_{fin})	6.5nm
Fin Height (H_{fin})	26nm
Effective Oxide Thickness (EOT)	0.85nm
STI/BOX Thickness	40nm
Fin Pitch (F_{pitch})	42nm
Gate Pitch	80nm
Metal1 Pitch	64nm

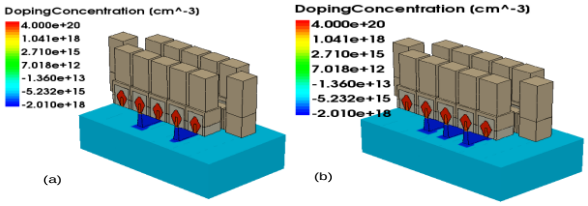

Fig. 1. 3D simulation structures of 2 different hybrid FinFETs. (a) SBSBS (b) SBBBS (S=SOI, B=bulk). STI/BOX and passivation layer are not shown in the figure.

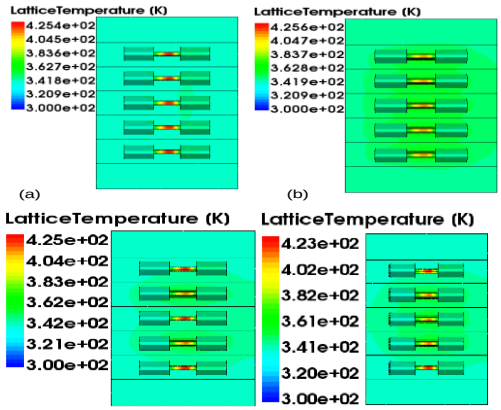

Fig. 2. Temperature distribution in different 5 fin hybrid FinFETs (Top view). (a) SSSSS (b) BBBBB (c) SBSBS (d) SBBBS

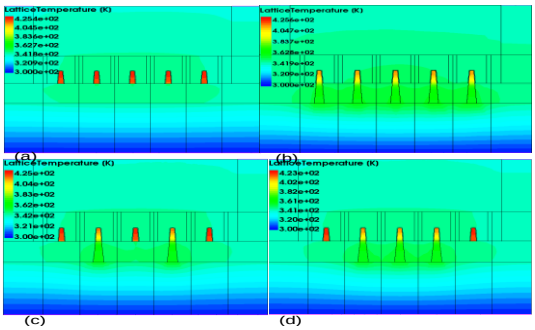

Fig. 3. Temperature distribution in different 5 fin hybrid FinFETs (Side view). (a) SSSSS (b) BBBBB (c) SBSBS (d) SBBBS

Table 2 I_{on}-I_{off} Characteristics (Vds,Vgs=0.8V)

Item	sssss	ssbss	sbsbs	sbbbs	bbbbb
I_{off} (nA/um)	100	100	100	100	100
I_{on} (uA/um)	820	816	812	805	801
% change in I_{off} (V_{sub}=-0.8)	--	6.2%	7.5%	9.5%	13.5%
% change in I_{on} (V_{sub}=-0.8)	--	0.3%	0.7%	1.1%	2.3%

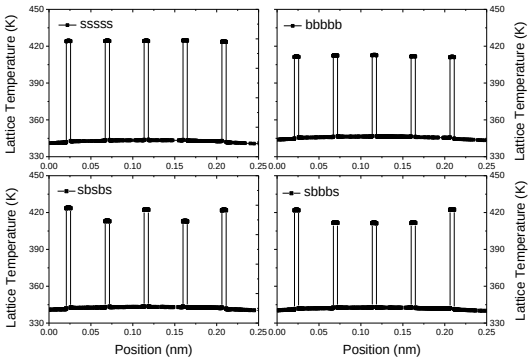

Fig. 4. Max. lattice temperature in the fins for different FinFET structures

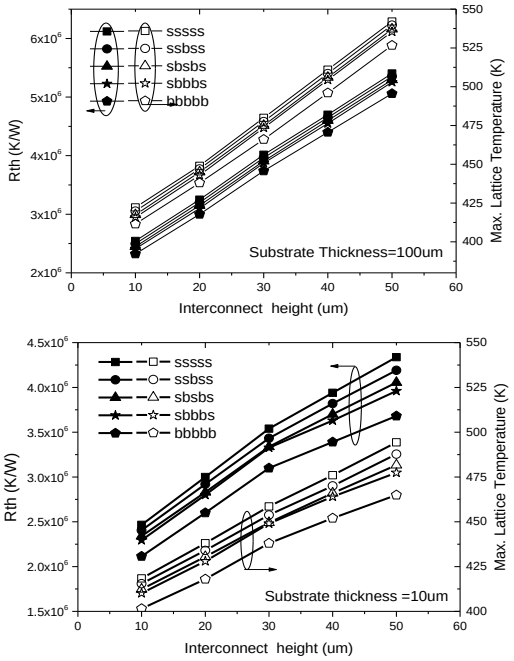

Fig. 5. Rth and Max. lattice temperature plot vs. interconnect height. (a) Substrate thickness=100um (b) Substrate thickness=10um

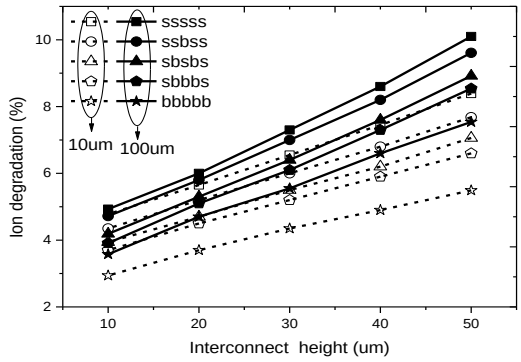

Fig. 6. Ion degradation vs. interconnect height for different substrate thicknesses.