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# Low Frequency Noise of Accumulation-Mode n- and p-MOSFETs fabricated on (110) Crystallographic Silicon-Oriented Wafers

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**Abstract**

**The paper investigates noise in accumulation-mode n- and p-MOSFETs on Si(110) wafers and demonstrates that using this new structure could be more advantageous than using the old one since the electrical performance of these transistors taken as complementary MOS are enhanced without any change in noise level other than an increase for the n-MOSFETs.**

## 1. Introduction

Strained technology is already employed by microelectronic manufacturers to enhance chips performances, and using new materials could further improve them. Germanium has greater mobility than Silicon, however Silicon is an abundant material and its extreme low cost technology is now very well established. Therefore, making use of a different crystallographic orientation like the (110) one, corresponding to a higher hole mobility, could be profitable [1]. Additionally, the introduction of a new MOS structure based on an accumulation layer rather than the inversion one could further improve chips performances by compensating the drop of drivability occurring on n-MOSFETs on Si(110) wafers [2]. Accumulation-mode MOSFETs on Si(110) wafers could ultimately achieve perfectly balanced CMOS for the next VLSI generation.

We propose here to evaluate noise performances of accumulation-mode n- and p-MOSFETs fabricated on (110) silicon-oriented wafers and investigate their noise sources.

## 2. Experiment and Results

Accumulation- and inversion-mode fully depleted n- and p-channel silicon-on-insulator (SOI) MOSFETs have been fabricated on bonded SOI (100) and (110) crystallographic silicon-oriented wafers. The process flow for all 33-mm-diameter wafers has been identical. The thickness of the SOI layer has been reduced down to 50 nm while its doping concentration has been adjusted by ion implantation to $10^{16}$ $cm^{-3}$, either acceptor or donor, depending on the desired type MOSFETs depicted in Figs. 1(a), 1(b), 1(c) and 1(d). The 7.5 nm-thick gate insulator has been fabricated by plasma oxidation. Electrical characteristics of accumulation- and inversion-mode n- and p-MOSFETs fabricated on Si(110) wafers is reported in Fig. 2 along with those of conventional MOSFETs on Si(100) wafers. With regards to inversion-mode transistors, the change from Si(100) wafers to Si(110) ones greatly improves the drivability of p-MOSFETs while it degrades that of n-MOSFETs. Indeed, as shown in Fig. 3, the hole mobility increases for Si(110) wafers while the electron one decreases. Nevertheless, the introduction of the accumulation-mode structure improves the drivability plotted in Fig. 2 of both n- and p-MOSFETs and can be further enhanced with an increase of the doping concentration of the SOI layer [3]. Indeed, as depicted in Figs. 1(a) and 1(c), an accumulation-mode MOSFET consists of a SOI layer doped like the contacts so that the drain current is the sum of a current generated by majority carriers accumulating inside a conductive layer located below the gate stack and a bulk current generated inside the neutral region of the SOI layer [3].

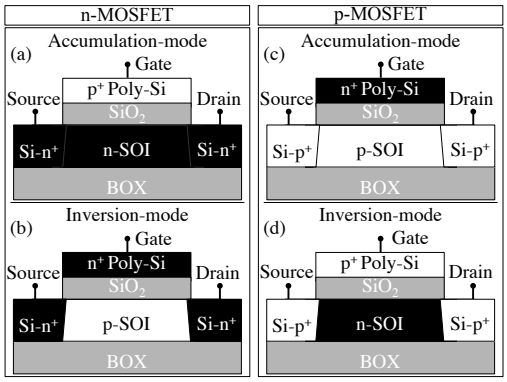


Fig. 1: Schematic of SOI accumulation- and inversion-mode n- and p-MOSFETs.

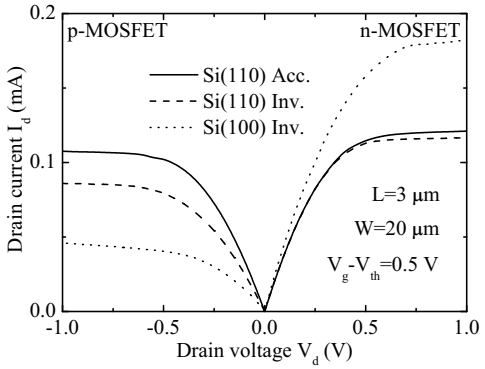


Fig. 2: Drain current versus drain voltage for SOI accumulation- and inversion-mode n- and p-MOSFETs when fabricated on (100) and (110) silicon-oriented wafers.

Noise of accumulation- and inversion-mode n- and p-MOSFETs fabricated on Si(110) and Si(100) are reported

respectively in Fig. 4 and Fig. 5. For either n- or p-MOSFETs, transistors on Si(100) wafers undoubtedly produce less noise and the origin of their noise is the sole fluctuations of the insulator charge [4].

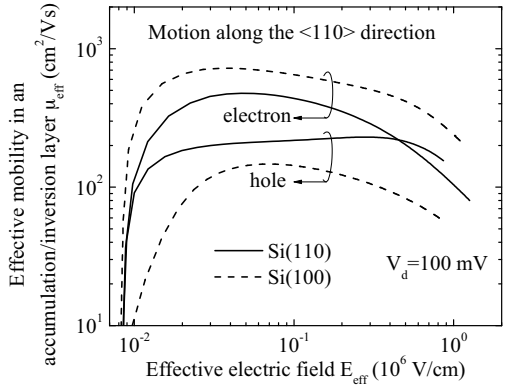


Fig. 3: Effective mobility versus effective electric field of hole and electron in an accumulation and inversion layer of MOSFETs fabricated on (100) and (110) silicon-oriented wafers. The channel is along the <110> direction.

With regards to Si(110) wafers at low bias, noise of accumulation- and inversion-mode MOSFETs is inversely proportional to the drain current, trend typical of noise stemming from the fundamental fluctuations of the mobility [5]. Furthermore, their level is almost identical, indicating that the Hooge parameter of the previous model is likely to be regardless if whether the conduction is occurring inside an inversion or accumulation layer. Still referring to Si(110) wafers, inversion-mode n-MOSFETs display a lower noise level than accumulation-mode n-MOSFETs while accumulation- and inversion-mode p-MOSFETs compare relatively well. Noise modeling of n-MOSFETs on Si(110) wafers is reported in Fig. 4 with the lines and has been carried out in the frame of the fluctuations of the insulator charge with induced mobility fluctuations [4].

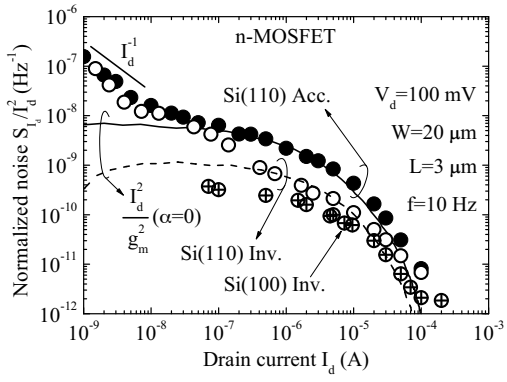


Fig. 4: Noise spectral density versus drain current of SOI accumulation- and inversion-mode n-MOSFETs when fabricated on (100) and (110) silicon-oriented wafers.

The Coulomb parameter α has been found equal to zero, indicating that there are no induced mobility fluctuations. Noise of accumulation- and inversion-mode n-MOSFETs on Si(110) wafers is stemming from the sole fluctuations of the insulator charge and consequently the lower noise of the inversion-mode MOSFETs is explained in terms of lower interface trap density. Noise modeling of accumulation- and inversion-mode p-MOSFETs on Si(110) wafers is reported in Fig. 5. It has been acknowledged a Coulomb parameter α different from zero, indicating that noise is originating from the fluctuations of the insulator charge and from the induced mobility fluctuations. The slightly lower level in favor of the inversion-mode p-MOSFETs is ascribed to its lower drivability. To finish, the increase of noise seen at high drain current is the evidence that noise stemming from the source and drain contact is taking over as the dominant noise source. This trend is not visible for n-MOSFETs in Fig. 4. Indeed, as shown in Fig. 3, surface roughness scatterings are limiting the mobility of electron earlier than that of hole [1], leading to deterioration of the drivability and in turns a suppression of noise stemming from the contatcs.

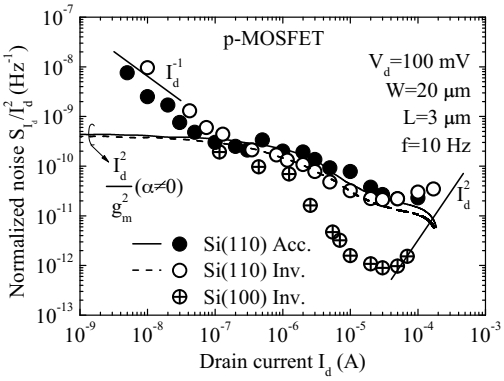


Fig. 5: Noise spectral density versus drain current of SOI accumulation- and inversion-mode p-MOSFETs fabricated on (100) and (110) silicon-oriented wafers.

## 3. Conclusions

There is no doubt that MOSFETs on Si(100) wafers produce the least noise but it can be beneficial for the drivability to use Si(110) wafers. In any case, accumulation-mode structures are worth introducing since they greatly enhance further electrical performances at the sole cost of an increase of the noise level in n-MOSFETs.


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