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Negative Bias Temperature Instability by Body Bias on Ring Oscillators in Thin BOX Fully-Depleted Silicon on Insulator Process

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Abstract

Body Bias (BB) control on Silicon On Insulator (SOI) mitigates power consumption on the stand-by mode. However, Negative Bias Temperature Instability (NBTI) changes by BB. We measure the NBTI of ring oscillators on thin buried oxide (BOX) fully-depleted SOI process. NBTI is suppressed and power consumption becomes lower by applying Reverse BB (RBB) because larger threshold voltage decreases carriers in channel when gate voltage is constant. Degradation rate of NBTI decreases by 23% and degradation factor decreases by 29% when RBB is applied from 0 to 1.0 V.

1. Introduction

In recent years, reducing power consumption is mandatory. Thin BOX fully-depleted SOI is one approach to operate in a low voltage of 0.4 V [1]. RBB can reduce power consumption further more. However, NBTI-induced degradation changes by BB [2]. NBTI is one of aging degradation and become significant concern in nano scaled devices [3]. Previous researches evaluated NBTI by BB when operating speed ($|V_{gs} - V_{th}|$) is constant [2]. When they measured in larger RBB, gate-source voltage (V_{gs}) increases. However, V_{gs} is usually constant and RBB is applied for lower power consumption. We measure NBTI by BB when V_{gs} is constant. We measure degradation of ring oscillators (ROs) by counting the number of oscillation in a short period between stress conditions.

2. BTI-induced Degradation

BTI is one of the aging degradations and V_{th} increases with time as voltage and temperature increase [3]. V_{th} increases when defects in a gate oxide trap carriers. It is explained by the atomistic trap-based BTI (ATB) model [4] as shown in Fig. 1. Each defect has a time constant by trapping carriers. BTI-induced degradation is in proportion to a logarithm according to the ATB model because time constants are uniformly distributed on the log scale between 10^{-9} and 10^{9} s [5]. BTI has a special feature of the recovery effect. V_{th} recovers when V_{gs} is removed because trapped carriers in the gate oxide are emitted to the channel.

There are NBTI (Negative BTI) and PBTI (Positive BTI). NBTI occurs in PMOS when V_{gs} is "0". Likewise, PBTI is observed in NMOS especially in technologies less than 45 nm with high-k gate dielectrics [6]. We consider only NBTI because our chip is fabricated in 65 nm.

NBTI is suppressed by RBB as shown in Fig. 2. V_{th} increases and carriers in channel decrease by applying RBB. Therefore, carriers are hardly trapped to the gate oxide as RBB increases.

3. Measurement Setup

We fabricated a chip including 11-stage ROs in a 65 nm process. The 11-stage RO is composed of NOR gates to dominate NBTI when ENB is high as shown in Fig. 3. PMOS of NORs are stressed by NBTI when ENB is high and ROs stop. When we measure frequencies, ENB becomes low only for 28 μs. BB changes from 0 V to 1.0 V. Fig. 4 shows a measurement flow. When the ROs oscillate, BB is 0 V to oscillate in the same condition. BB is applied when the ROs stop. In this time, ROs suffer from NBTI and are in a low-power mode when RBB is applied.

Fig. 5 shows the test chip fabricated in a 65 nm thin BOX fully-depleted SOI process. The chip has 576 ROs of same structure. It can change the BB through the 10 nm BOX layer.

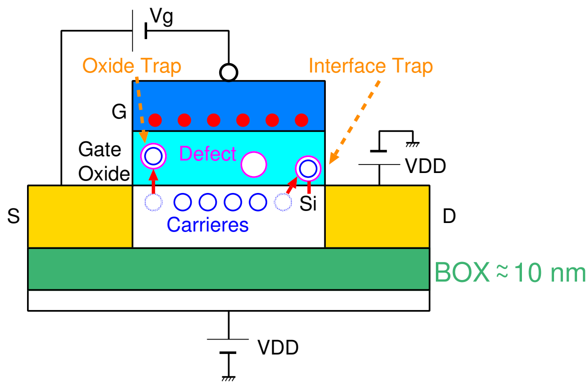

Fig. 1. Atomistic trap-based BTI (ATB) model.

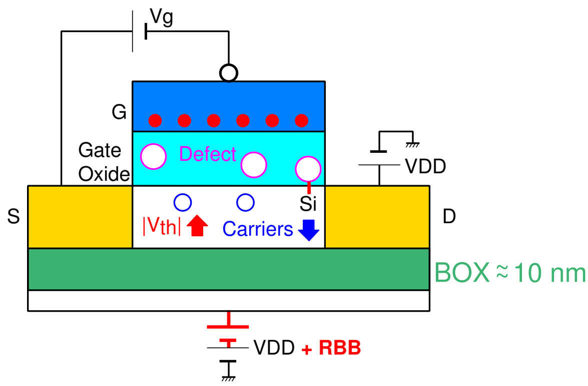

Fig. 2. Suppression of NBTI by reverse body bias (RBB).

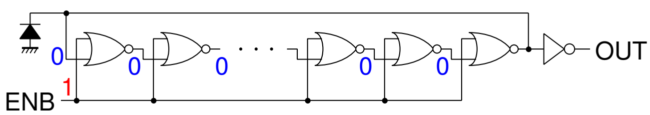

Fig. 3. 11-stage ring oscillator.

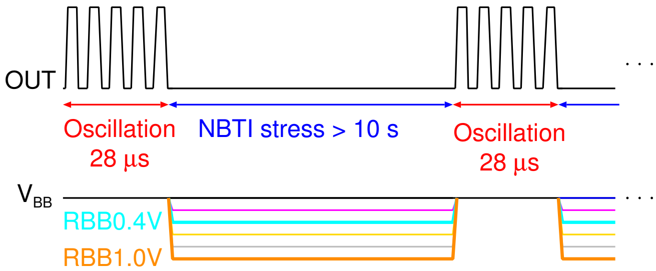

Fig. 4. Measurement flow.

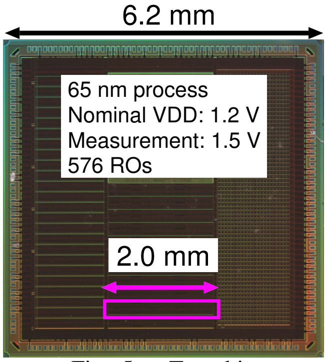

Fig. 5. Test chip.

4. Measurement Results

We measured initial frequencies before NBTI measurement to confirm recovery effect of NBTI. If those are different, NBTI-induced degradation remains. Fig. 6 shows measurement results of initial frequencies. Initial frequencies are 1.57 GHz after stressing ROs by RBB 7 times from 0 to 1 V. It means NBTI-induced degradation does not remain before measuring in each condition.

NBTI measurement condition is at 80 °C and 1.5 V to accelerate BTI degradation by the temperature and the voltage. Fig. 7 shows NBTI measurement results by changing the body bias. X-axis is stress time and Y-axis is degradation rate based on initial frequencies. Dots represent average of measurement data and line is drawn by the fitting function of Eq. (1).

$$S_{\mathrm{NBTI}} \log(t+1) \tag{1}$$

S_{NBTI} is a fitting parameter indicating degradations caused by NBTI. This function comes from the ATB model since defects have a time constant distributed uniformly on the log scale from 10^{-9} s to 10^{9} s. Fitting functions are drawn along the measurements as shown in Fig. 7. The ATB model replicates NBTI-induced degradations. Degradation rate decreases as RBB increases. NBTI-induced degradation is suppressed by applying RBB. Degradation rate decreases by 23% applying RBB from 0 to 1.0 V. We also evaluate degradation factor S_{NBTI}. Fig. 8 shows the degradation factor S_{NBTI}. It also decreases as RBB. S_{NBTI} decreases 29% by applying RBB from 0 to 1.0 V. RBB suppresses NBTI-induced degradation and also makes power consumption lower.

5. Conclusion

We fabricated ring oscillators in 65 nm thin BOX fully-depleted SOI process and measured their frequencies to evaluate NBTI by body bias. NBTI is suppressed when Reverse Body Bias (RBB) is applied because carriers in channel decrease. Degradation rate decreases by 23% from no RBB to RBB $=$ 1.0 V. Degradation factor which comes from fitting

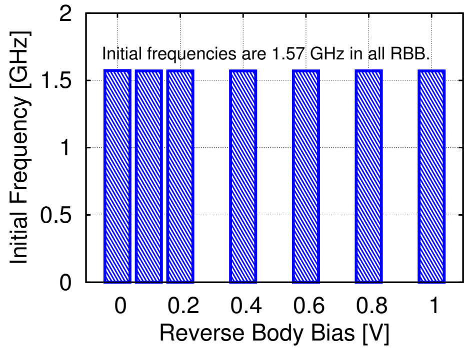

Fig. 6. Initial frequencies in all of the body bias conditions.

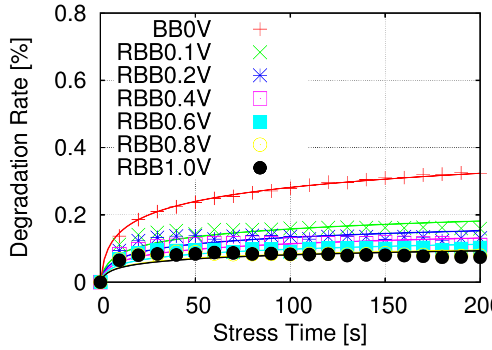

Fig. 7. Measurement results of NBTI by body bias.

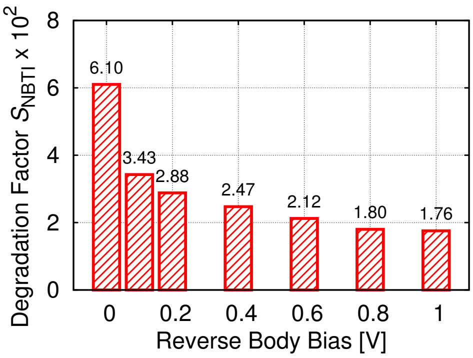

Fig. 8. Degradation factor S_{NBTI} from fitting function.

function decreases by 29% in the same condition. Applying RBB is a helpful technique for lower power consumption and suppress NBTI.

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References

[1] R. Tsuchiya et al., *IEDM*, pp 631-634, 2004.
[2] J. Franco et al., *IEDM*, pp 18.5.1-18.5.4, 2011.
[3] V. Huard et al., *IRPS*, pp 289-300, 2008.
[4] H. Kukner, et al., *IEEE Trans. on Dev. & Mat. Rel.*, vol. 14, pp. 182-193, 2014.
[5] B. Kaczer et al., *IRPS*, pp XT.3.1-XT.3.5, 2011.
[6] S. Zafar et al., *VLSI Tech.*, pp. 23-25, 2006.