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Compact Model of FeFET Memory Based on Multi-Domain Landau-Khalatnikov Theory

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We report a newly developed FeFET compact model based on the time dependent Landau-Khalatnikov (LK) theory. In this model, a multiple ferroelectric domain structure which can be thermally activated is taken into account. We demonstrate that the device characteristics of FeFETs reported in experiments are well fitted by our compact model. We also perform the circuit simulation for the inverter utilizing FeFETs by using this compact model. Unlike normal inverters composed of the MOSFETs, the switching speed of the inverter changes with the voltage pulse before the operation.

1. Introduction

In recent years, a nonvolatile memory, which requires no refresh operation, has attracted much attention as a novel storage with low-power consumption. Moreover, the non-volatile memory which shows analog response, such as "memrister" [1], is expected to be a fundamental component of neuromorphic computer. The one transistor type nonvolatile memory based on ferroelectric-gate field-effect transistor (FeFET) operates with nondestructive readout and shows extremely low power consumption [2]. FeFET memory also has a high scalability and a high endurance, and the 100 nm gate length with 10^8-cycle endurance has been achieved [3]. Moreover, FeFETs show analog-like response to the applied gate voltage [4]. Thus, their characteristics have received much attention from the viewpoint of nm-scale neuromorphic circuit [5]. However, the lack of reliable compact model of the FeFETs makes it difficult to study novel circuit applications utilizing FeFETs.

In this work, we develop the compact model of FeFETs which reproduces device characteristics reported in an experimental study. We perform the simulation for a simple inverter circuit composed of FeFETs, and confirm that this compact model running well on the circuit simulator, SmartSpice [6].

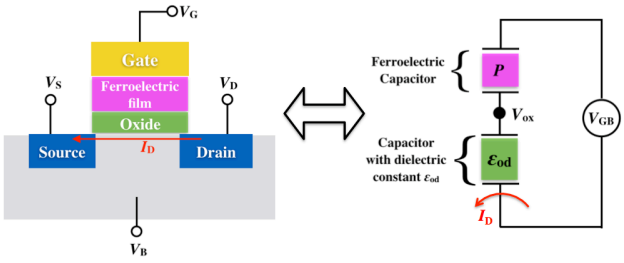

Fig. 1. Schematic figure of FeFET with MIFS stack (Left), and an equivalent circuit model for the FeFET (Right).

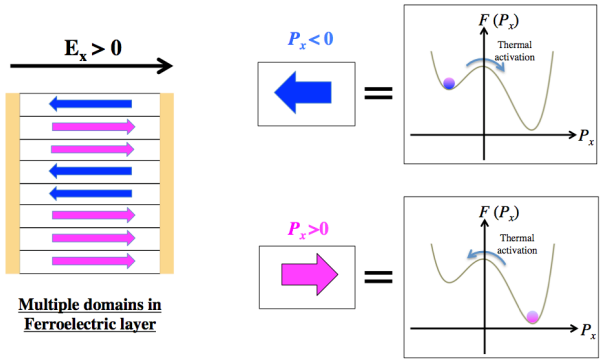

Fig. 2. Schematic figure of multi-domain model for the ferroelectric layer.

2. Modeling

We focused on the most successful FeFETs at this stage composed of metal-ferroelectric-insulator-semiconductor (MFIS) stack [3,4] shown in the left side of Fig. 1. In this device, a bias voltage applied to the gate induces dielectric polarization in the ferroelectric layer. The residual polarization changes the effective voltage applied to the oxide layer, and thus changes the threshold voltage V_{th}. Since the value of residual polarization depends on the record of the applied voltage before the operation, the shift of V_{th} can be used as nonvolatile memory.

In order to describe the above situation, we considered equivalent circuit model consisting of two capacitors connected in a series as shown in the right side of the Fig. 1. One is the capacitor corresponding to the ferroelectric layer, and the other is the capacitor corresponding to the oxide layer. The equation for the circuit is given by

$$V_{GB} = d_F\left(\frac{\sigma_Q}{\epsilon_0} - \frac{\overline{P}}{\epsilon_0}\right) + d_{ox}\frac{\sigma_Q}{\epsilon_{ox}}, \qquad (1)$$

where ε_0 and ε_{ox} are dielectric constant of the free space and the oxide, d_F are d_{ox} the thickness of the ferroelectric layer and the oxide layer, $\overline{P}$ is the averaged polarization in the ferroelectric layer, σ_Q is the charge density of the capacitors, and V_{GB} is the bias voltage between the gate and the base. Regarding the dynamics of the polarization, we focused on the component of the polarization parallel to the electric field applied to the ferroelectric layer, P_x.

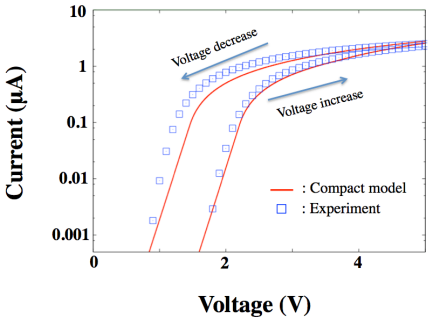

Fig. 3. I_D-V_{GS} curves in the experiment [4], and in our compact model.

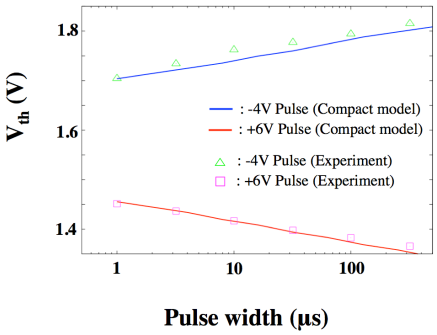

Fig. 4. V_{th} as a function of the width of the voltage pulse in the experiment [4], and in our compact model.

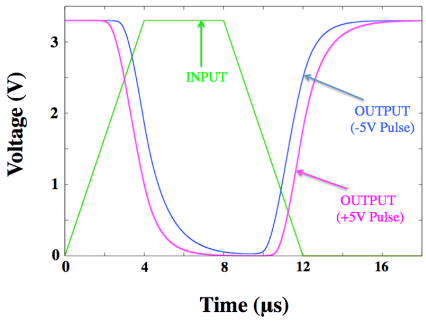

Fig. 5. Operation of the inverter composed of FeFETs after the application of the voltage pulse, +5 V and −5 V.

The time evolution of P_x based on the LK theory is described as [7]

$$\frac{1}{D}\frac{dP_x}{dx} = -\frac{dF}{dP_x} = -2\alpha P_x - 4\beta P_x^3 + E_x, \qquad (2)$$

where D is the diffusion constant, α and β are the parameters specifying the properties of the ferroelectric polarization, and E_x is the electric field applied to the ferroelectric layer. For describing the properties originating from the multiple-ferroelectric domain structure, multiple P_x's corresponding to the number of the domain N_D were considered. We assumed that the dynamics of these P_x's is described by similar equations shown in Eq. (2), however, they can flip their polarity independently by thermal activation. Figure 2 shows the schematic figure of our multi-domain model for ferroelectric layer. In order to implement this model into circuit simulators by using Verilog-A language [8], we simply treated the two equations representing the plus and the minus polarity, P_{x+}, P_{x-}. The averaged polarization is given by $\bar{P} = (N_{D+}P_{x+} + N_{D-}P_{x-})/N_D$. The number of the plus and the minus polarity, N_{D+}, N_{D-}, change with the time and the electric field E_x accoding to the activation rate, $\omega_p \exp(-(U_P - \gamma E_x) / k_B T)$, where ω_p is the trial frequency, U_P is the activation energy, γ is the parameter which describes the decrease (increase) of the activation energy by the applied field, k_B is the Boltzman constant, and T is the temperature.

3. Results

First, we calculated device characteristics of the FeFET using the circuit simulator, SmartSpice, and compared with the experimental results. Figure 3 shows the examples of the I_D-V_{GS} curves reported in Ref. [4] and those of our compact model. This figure indicates that V_{th} changes with the direction of the voltage sweep, and our results shows good agreement with experimental results. Figure 4 shows the V_{th} of the same devices as a function of the width of the voltage pulse which is applied before the operation. It is seen that experimental results are also fitted well by those of our compact model. In this figure, we can see that the V_{th} linearly increases (decreases) with respect to the logarithm of the width of the negative (positive) pulse. This peculiar feature is attributed to the negative feedback on the thermal activation. The flip of the polarization by thermal activation reduces the electric field E_x, and this results in the decrease of thermal activation rate itself.

Finally, we performed circuit simulation of the inverter composed of an n-type FeFET and a p-type FeFET. The operation voltage V_{DD} is 3.3 V. We apply voltage pulse V_x = +5 V (−5 V) with 10 μs width before the operation. Figure 5 shows the characteristics of the output V_z for trapezoidal input V_x. As indicated in this figure, the switching time changes with the initial pulse polarity which causes V_{th} shift. Such tunability will be helpful for the design of a high speed and low power consumption circuit.

4. Conclusion

In this paper, the compact model of the FeFETs with MFIS stack has been developed. The dynamics of the dielectric polarization in the FeFETs is calculated based on the LK theory taking into account the multiple ferroelectric domain structure. Our compact model implemented in the Verilog-A language reproduces well the characteristics of the FeFET reported in the experimental study. By using this compact model, we have performed the simulation of the inverter circuits composed of FeFETs and shown that the switching speed of the inverter is controlled by the voltage pulse.

Acknowledgements

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