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Enhanced Operation Characteristics in Poly-Si Nanowire Charge-Trapping Flash Memory Device with Ge Buried Channel

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Abstract

Operation characteristics of polycrystalline silicon (poly-Si) nanowire (NW) charge-trapping (CT) flash memory devices with SiGe and Ge buried channel are studied and compared in this work. The CT flash devices with Ge buried channel show faster programming and erasing speeds as compared to those with SiGe one due to a lower energy barrier in tunneling layer with more Ge composition. The retention and endurance characteristics of devices with Ge buried channel are similar to those with SiGe one. Thus, Ge buried channel is promising to CT flash device for 3D nonvolatile memory applications.

1. Introduction

With increasing the demand of high density nonvolatile memory, polycrystalline silicon (poly-Si) is an attractive device channel for three-dimensional (3D) charge-trapping (CT) NAND flash device. By introducing nanowire (NW) configuration, operation speed can be improved due to the enhanced electrical field by curvature of NW [2]. Recently, some efforts about the utilization of SiGe buried channel have been reported to improve P/E speeds [3]-[5]. The improvement is resulted from the fact that more carriers are generated by the smaller bandgap of SiGe during P/E operations [3]-[5]. Also, effects of SiGe buried channel on poly-Si NW flash memory device has been studied in our previous work [6]. Faster P/E speeds are achieved with increasing Ge contents in SiGe buried channel. To further improve operation characteristics, effects of Ge buried channel on poly-Si NW CT flash device are studied in this work. Operation and reliability characteristics of devices with SiGe and Ge buried channels are investigated and compared.

2. Devices fabrication

Poly-Si NW flash devices with Ge and SiGe buried channel are both fabricated on 6-inch Si wafers. A 200-nm thick SiO_2, a 50-nm thick Si_3N_4 buried layer and an 100-nm thick SiO_2 are sequentially deposited by low-pressure chemical vapor deposition (LPCVD) systems. The NW and active region formation processes are reported as our previous work [6]. Samples for Ge and SiGe buried channel devices are then sent to grow a 5-nm thick epitaxial Ge/SiGe (with 30 % Ge contents) layer and a 3-nm thick Si-cap layer, respectively, by an ultrahigh-vacuum chemical molecular epitaxy (UHVCME) system [5]. Note that the Ge, SiGe and Si-cap layers are only grown on the surface of active region due to the high selectivity of epitaxy. Then, both samples are sent to form dielectric and gate layers. A 5-nm thick SiO_2 is grown as tunneling layer at 1000 °C for 50 s by a rapid thermal oxidation (RTO) process. Then, 4-nm thick HfAlO and 4-nm HfO_2 stacked CT layer are deposited by an atomic layer deposition (ALD) system; an 17-nm thick Al_2O_3 is also deposited as blocking layer by ALD system. The rest processes are also the same as those in [6]. Since a high temperature may increase Ge diffusion and degrade dielectric quality, all the processes after UVHCME epitaxy are performed under 600 °C.

3. Results and Discussion

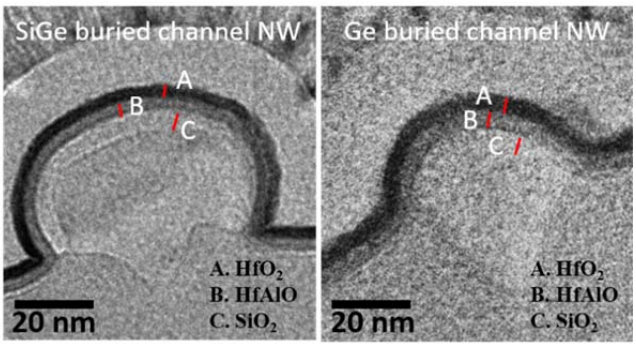

Fig. 1 Cross-section TEM images of NW with (a) SiGe buried channel and (b) Ge buried channel.

Fig. 1 shows cross-section image of SiGe and Ge buried channel NW by transmission electron microscope (TEM). The width of SiGe and Ge buried channel NW are about 40 nm and 38 nm, respectively. The Id-Vg characteristics at drain voltage (V_{DS} = 0.5 V) of CT flash devices with SiGe and Ge buried channel are shown in Fig. 2. Both devices show similar transfer characteristics and I_{on}/I_{off} ratios are all about 10^6.

The programming/erasing (P/E) operations in this work are all performed by the Fowler–Nordheim (FN) tunneling mechanism. Fig. 3 shows (a) programming and (b) erasing speed of SiGe and Ge buried channel device at the gate voltage (V_{GS}) of ±16 V, respectively. The threshold voltage shift (ΔV_{th}) refers to those of erase state. With more Ge content in buried layer, the Ge buried channel device shows faster programming speed than SiGe one. This may be because the Ge buried channel device has more Ge content near tunneling layer as compared to the SiGe one. The ef-

fects of lower energy barrier in tunneling layer are more obvious for Ge channel device [7]. As for the erasing speed, the Ge buried channel device shows faster erasing speed than SiGe one due to more Ge content in buried layer. Note that both devices are programmed at V_{GS} = 16 V for 1 s before erasing speed measurements. The ΔV_{th} value refers to those of program state.

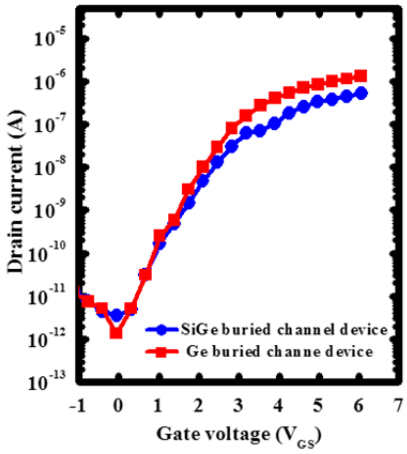

Fig. 2 Id-Vg characteristic of SiGe and Ge buried channel devices.

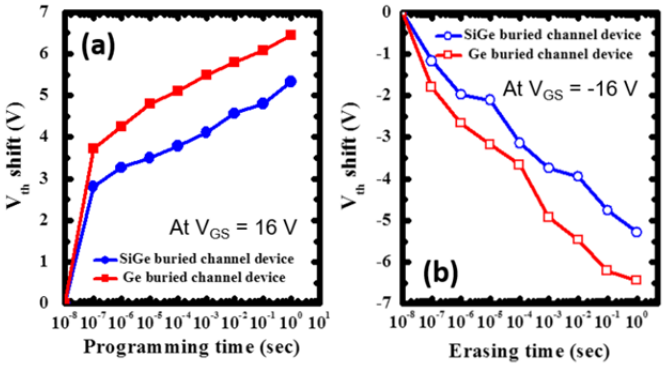

Fig. 3(a) Programming and (b) Erasing speed of SiGe and Ge buried channel devices.

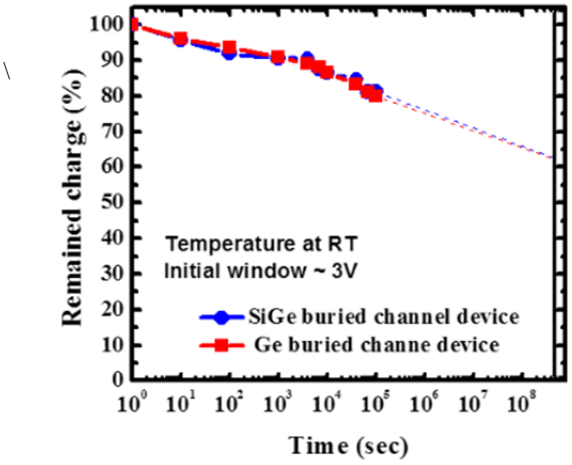

Fig. 4 Retention characteristics of SiGe and Ge buried channel devices.

Fig. 4 shows retention characteristics of SiGe and Ge buried channel devices. Both devices are programmed for 3 V memory window and tested at room temperature (RT). The retention performance of SiGe and Ge buried channel device are very similar. This is because the possible Ge diffusion from Ge buried channel is minor, and all the dielectrics between channel and gate pad are the same.

The endurance characteristics of SiGe and Ge buried channel devices are shown in Fig. 5. With the same memory window, SiGe and Ge buried channel devices keep a large memory window of ~3 V even after 10^5 P/E cycles. Therefore, operation speeds of CT flash devices with Ge buried channel can be further improved, and reliability characteristics are also comparable.

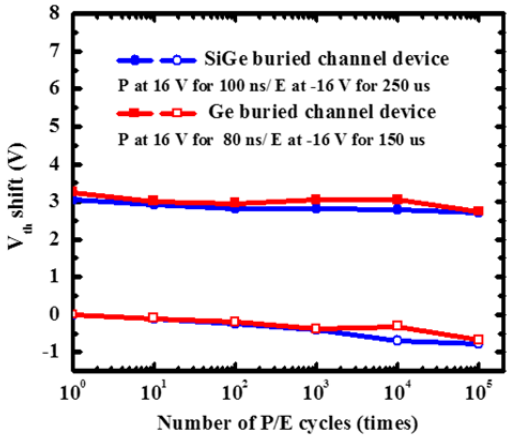

Fig. 5 Endurance characteristics of SiGe and Ge buried channel devices.

4. Conclusions

Operation characteristics of poly-Si NW CT flash devices with Ge and SiGe buried channel are investigated and compared in this work. Operation speeds of CT flash memory devices can be further improved by a Ge buried channel, while good reliability characteristics are retained, Indicating the Ge diffusion from Ge buried channel into tunneling oxide is minor. Therefore, Ge buried channel is promising to improve operation characteristics of CT flash devices for 3D integrations.

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