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# Enhanced Retention Characteristics in Double Gate Tunnel FET based DRAM

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**Abstract**

**The work presents an innovative approach to enhance retention time in sub-100 nm Double Gate (DG) Tunnel Field Effect Transistor (TFET) by optimally controlling the lateral spacing, misalignment, and underlap between front and back gates. The front gate primarily regulates read mechanism based on Band-to-Band Tunneling (BTBT) and non-self aligned back gate creates a deep physical well. Along with the deep potential well that sustains holes for longer duration, an underlap region at the back gate/drain junction controls BTBT which improves the retention time. The use of a lateral separation between the gates increases the effective length of the storage region, which along with an underlap region (20 nm) and optimal biases enhances the retention time to 550 ms at 85 °C for a device with a front gate length of 100 nm.**

## 1. Introduction

Tunnel Field Effect Transistors (TFETs) have attracted significant attention due to the sharp switching from the off-to-on state [1-4]. Initial TFET design for dynamic memory in Silicon-on-Insulator (SOI) technology focused on the use of the back gate or an implanted $p^+$ region to achieve memory characteristics, but with a retention time lower than 64 ms [2-4]. Other $p^+$-i-$n^+$ devices such as Zero-slope and Zero-impact ionization FET ($Z^2$-FET) [5-7] and Field Effect Diode (FED) [8-9], operating in forward bias mode have achieved good retention characteristics in comparison to TFETs, which operate in reverse bias and have previously reported a retention time in few milliseconds at room temperature [3]. In this work, through an insightful analysis, we focus on developing a methodology to improve the retention time and scalability of Double Gate (DG) TFETs. The retention time of ~ 550 ms is achieved at 85 °C with a gate and storage region length of 100 nm.

## 2. Results and discussion

The device analysis has been carried out using ATLAS simulation tool [10] using the models well calibrated to the available experimental data [1] for TFETs (Fig. 1*a*-*b*). The non-local model simultaneously with Klaassen model for Band-to-Band Tunneling (BTBT) along with band gap narrowing, Shockley-Read-Hall recombination model with Scharfetter relation (with $\tau_{max}$ = 100 ns, $\tau_{min}$ = 0 ns, $N_{reff}$ = 5 x $10^{16}$ $cm^{-3}$ and $\gamma$ = 1) [9-10] and Lombardi mobility model were used [10]. Fermi statistics, and temperature dependent lifetime [11] was used in the analysis.

The key to the device functionality is the different roles of the front and back gates, with each ideally controlling a separate region of the semiconductor film. Hence, gate misalignment possible through shifting of electric vernier [12] and as shown in Fig. 2*a*, is incorporated in the design. The work focuses on utilizing a lateral separation between the gates ($L_{gap}$) and an underlap ($L_{un}$) between the back gate and drain, which allows the gate length ($L_{g2}$) to be scaled down to 25 nm.

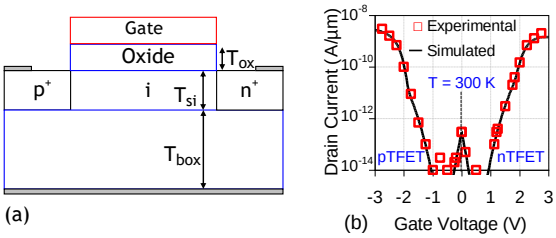


Fig. 1: (a) Schematic diagram of Tunnel FET. (b) Comparison of drain current ($I_{ds}$) - gate voltage ($V_{gs}$) characteristics of TFET of our simulations with experimental data [1]. Parameters: $L_g$ = 400 nm, $T_{si}$ = 20 nm, $T_{ox}$ = 3 nm ($HfO_2$), $T_{box}$ = 145 nm, and $|V_d|$ = 1 V.

The $n^+$ poly front gate ($L_{g1}$ = 100 nm) governs the read mechanism based on band-to-band tunneling and is aligned towards source at a partial portion of intrinsic region while the $p^+$ poly back gate ($L_{g2}$ = 100 nm) positioned beneath the front un-gated region creates a dedicated volume for charge storage. Without requirement of a precise doping of p-region [4], the use of misaligned $p^+$ poly back gate creates a physical well (Fig. 2*b*) which is more profound than that formed using a conventional back gate [2-3]. The misalignment traditionally considered as a drawback due to loss of gate controllability is beneficial in preserving a deeper potential well in the proposed architecture. Apart from deeper well, a wider storage region (Fig. 2*c*) is achieved primarily through a combination of $L_{gap}$ and $L_{g2}$. The deep potential well with an optimised set of bias values (Fig. 3*a*) maintains holes for longer duration, maintaining state '1'and thereby improving the Retention Time (*RT*). However, state '0' is degraded (Fig. 3*b*) due to thermal generation and BTBT [13], which determines *RT*. The retention time can be further improved by preserving state '0' for a longer duration which is achieved using a gap ($L_{gap}$) between the front gate and back gate, and an underlap ($L_{un}$) between the back gate and drain.

Fig. 4 shows the improved performance metrics in terms of *RT* for device with $L_{gap}$. The difference between read currents for state '1' ($I_1$) and '0' ($I_0$) is estimated as Sense Margin (*SM*) and the time required to reduce the maximum sense margin ($\Delta I$) by 50% is assessed as Retention Time (*RT*) [13]. The wider storage area due to $L_{gap}$ and $L_{g2}$ preserves the charges for longer duration. Although state '1' is already maintained due to deep physical well along with an

optimised bias of -0.2 V at the back gate during hold state, the wider well aids to sustenance of state '0'. While the *RT* is enhanced to 250 ms with the introduction of an $L_{gap}$ (50 nm) between the gates (Fig. 4), *SM* is unaltered in comparison to Case-I with a *RT* of 80 ms (fig. 3*a*).

An optimised underlap (20 nm) decreases the BTBT of electrons into drain due to reduced lateral electric field, leading to a slower decay of state '0' and thus, improved retention characteristics (~550 ms) at 85 °C (Fig. 5). The write '1' operation is also based on the back gate/ drain tunneling which along with an underlap region result into reduced hole accumulation in the storage region. This results into reduced read current '1', thereby decreasing the sense margin. Although with $L_{un}$ TFET suffers from reduced *SM*, it shows high retention characteristics even at scaled lengths. The back gate can be scaled down to 25 nm with $L_{g1}$ = 100 nm, achieving *RT* > 64 ms and *SM* maintained (30-40 nA) at 85 °C (Fig. 6). This is significantly better than the previous results that achieved *RT* of ~100 µs at 85 °C with $L_{g1}$ = 100 nm and $L_{g2}$ = 25 nm [4], and few milliseconds at 27 °C for the gate length of 400 nm and storage region of 200 nm [3]. The progress in retention time with respect to other TFET based DRAM has been illustrated in Fig. 7. The optimized use of biases, underlap and gap has shown remarkable improvement in *RT* for scaled lengths. Thus, with proper design of device architecture, our TFET based DRAM shows an enhanced retention time with better scalability.

## 3. Conclusion

The present work demonstrates an optimal design of TFET that highlights enhanced retention time and better scalability as compared to the previous TFET based DRAM. Gate misalignment coupled with back gate-to-drain underlap and gap between the gates along with appropriate biases is critical for enhanced performance to achieve a retention time of ~ 550 ms at 85 °C. The device design incorporated with these features also permits the storage region to be scaled down to 25 nm.


## Acknowledgements

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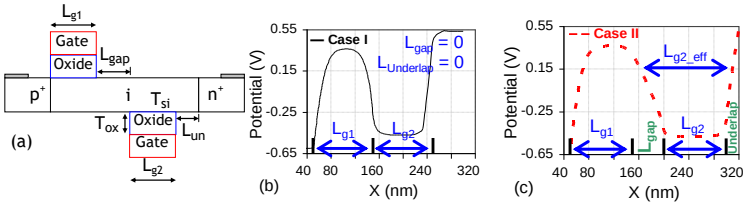


Fig. 2: (a) Schematic diagram of a misaligned Double Gate (DG) MOSFET with gap between the gates ($L_{gap}$) and an underlap ($L_{un}$) region between the back gate and drain. Variation of electrostatic potential for the case (b) without (Case I) and (b) with (Case II), $L_{gap}$ and $L_{un}$ regions. Parameters: $L_{g1}$ = $L_{g2}$ = 100 nm, $T_{si}$ = 20 nm, $T_{ox}$ = 3 nm ($HfO_2$), $L_{gap}$ = 50 nm, $L_{un}$ = 20 nm, Source/Drain doping = $10^{20}$ $cm^{-3}$.

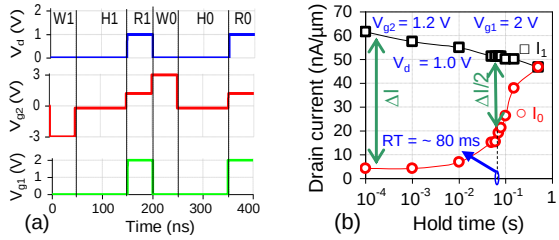


Fig. 3: (a) Programming scheme in the sequence of operation. (b) Read currents for Case-I. W, H, and R indicate the write, hold, and read operation, respectively. $V_{g1}$, $V_{g2}$, and $V_d$ are the voltages applied at the front gate, back gate and drain, respectively.

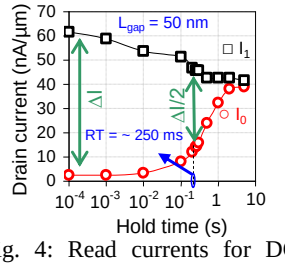


Fig. 4: Read currents for DG TFET with a gap ($L_{gap}$) between the front and back gate.

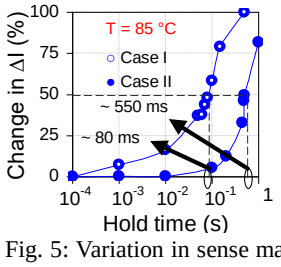


Fig. 5: Variation in sense margin with time for Case-I, and Case-II, *RT* estimated when the maximum *ΔI* is changed by 50%.

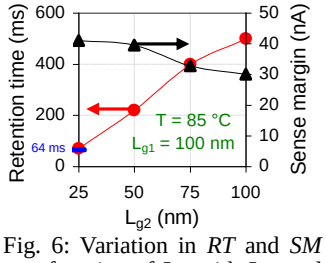


Fig. 6: Variation in *RT* and *SM* as a function of $L_{g2}$ with $L_{gap}$ and $L_{un}$ regions.

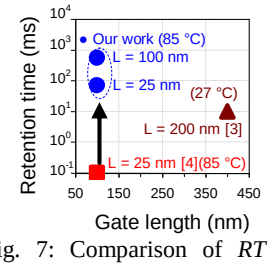


Fig. 7: Comparison of *RT* of various TFET based DRAM as a function of $L_{g1}$. *L* indicates length of the storage region.