Extended Abstracts of the 2016 International Conference on Solid State Devices and Materials, Tsukuba, 2016, pp741-742

PS-4-10(Late News)

One-Transistor Ferroelectric Versatile Memory with Multi-Level Operation

Yu-Chien Chiu[1], Yu-Wen Hung[2], Chia-Chi Fan[1], Chien Liu[2], Wen-Wei Lai[1], Yi-Ru Chen[1], Po-Wei Chen[3], *Chun-Hu Cheng[3], #Chun-Yen Chang[1] and Wu-Ching Chou[2]

[1] Dept. of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan
#Phone: +886-3-5712121#59318 E-mail: cyc3562@gmail.com
[2] Dept. of Electro-physics, National Chiao Tung University, Hsinchu, Taiwan
[3] Dept. of Mechatronic Engineering, National Taiwan Normal University, Taipei, Taiwan
*Phone: +886-2-7734-3514 E-mail: chcheng@ntnu.com.tw

Abstract

This paper described the memory characteristics of the one-transistor (1T) ferroelectric versatile memory under multi-level operation. The multi-level operation characteristics are evaluated at a fast 100ns and low program/erase voltages of 6V. The district V_T level and stable memory window has been confirmed at different memory states with low-voltage pulse-triggered configurations, which appears very attractive for ultralow-power memory application.

1. Introduction

Recently, the studies of ferroelectric transistor and memory attract more attention due to the finding of highly scalable hafnium-based ferroelectric materials. However, the strong depolarization field of ferroelectric domain plays a crucial role for the application of nonvolatile memory. Our versatile memory with an additional functional integration of charge trapping property had been demonstrated to significantly improve the nonvolatile memory characteristics [1]-[5]. Our 1T ferroelectric versatile memory reached the steep sub-60 mV/dec switching and fast program/erase speeds (sub-100ns) that were more favorable to reduce the dynamic power consumption. After confirming the memory properties and switching mechanism, we intend to investigate the possibility of multi-level operation. Therefore, the stability of V_T level at low program/erase pulse voltage and the switching reliability of memory window under long endurance cycles will be investigated in this work.

2. Device Fabrication

The schematic view of developed versatile memory was shown in Fig. 1. A novel versatile memory has been demonstrated in *p*-MOSFET by employing ferroelectric HfZrO and charge-trapped ZrSiO layers. Then fabrication process of *p*-type ferroelectric MOSFET was simply described below. First, a 3.5-nm SiO_2 was grown as a buffer oxide and followed by the deposition of 20-nm-thick HfZrO and 5-nm-thick ZrSiO and 400°C PDA. Subsequently, the ~3-nm SiO_2 was deposited as a top tunnel oxide. After pattering a TaN gate electrode, self-aligned BF^{2+} was implanted and activated by a RTA. Finally Al metals were formed as source/drain contacts.

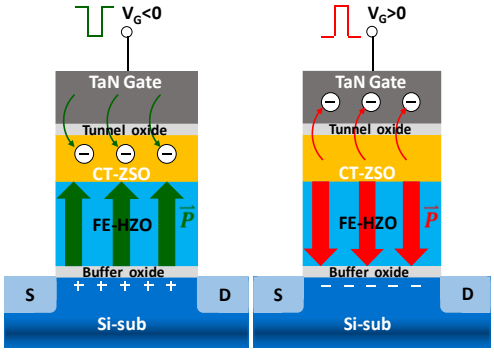

Fig. 1 Schematic plot of memory operation of one-transistor ferroelectric versatile memory.

3. Results and Discussion

Fig. 2 shows a V_T shift (ΔV_T) of 3 V under +6/-6V voltage sweeping. The large ΔV_T window and steep turn-on transistor characteristic are mailny attributed to the fast ferroelectric domains switching and strong polarization with the assistance of vertical electric field of charge trapping layer of ZrSiO. According our recent simulation, the ferroelectric polarization effect of hafnium-based dielectric is also determined by phase transformation process (from metastable monoclinic to orthorhombic) and the change of delocalized D-states that are originated from thermal strain effect of metal gate [4].

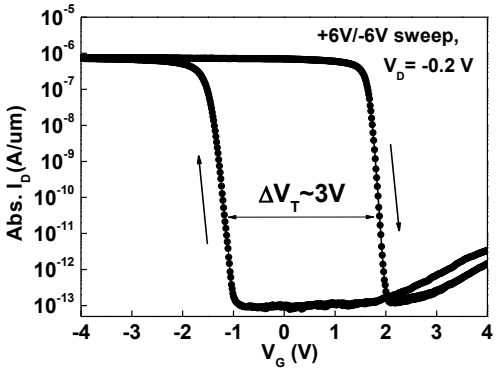

Fig. 2 I_D-V_G characteristics of ferroelectric versatile memory.

The endurance characteristics of the 100-ns pulse width is shown in Fig. 3. The fast V_T shift is clearly observed under a 100ns pulse speed while negative program voltage

of –6V and positive erase voltage of +6V were applied. The stable V_T shift and memory window can be maintained even up to 10^{12} times. The slight V_T variation under long endurance cycling may be caused by discrete trapping levels near CT-ZSO/FE-HZO interface that cannot be ruled out during fast-speed pulse operation [5], as shown in Fig. 4. In Fig. 5, the fast drain current response under 100ns is measured and further confirmed by applying a smaller program voltage of -3V and reading voltage of +0.3V.

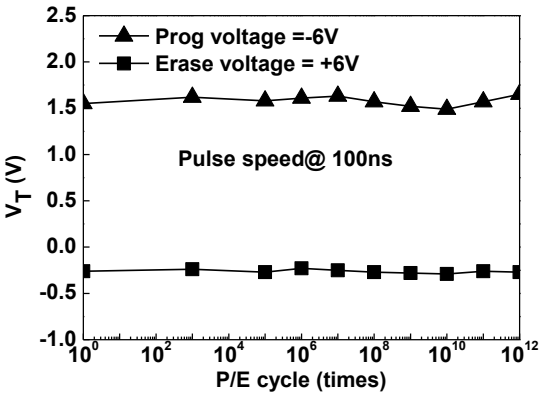

Fig. 3 Endurance of ferroelectric versatile memory measured at a pulse of 100ns.

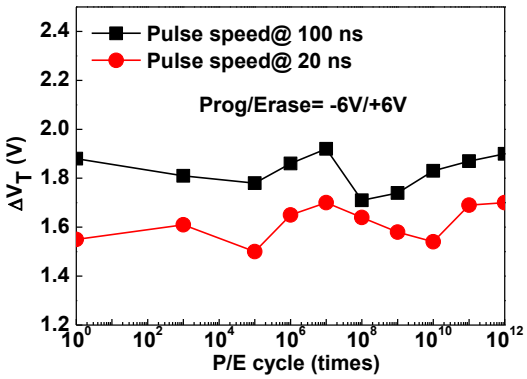

Fig. 4 ΔV_T as a function of P/E cycles under 20ns and 100ns pulse speed.

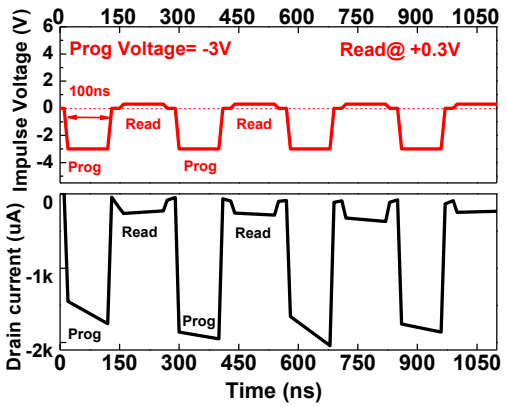

Fig. 5 Impulse pulse voltage of -3V (+0.3V reading voltage) and corresponding current response.

Fig. 6 shows the characteristic of the tunability of V_T shift under the program/erase voltages of 3~7 V with a 100ns pulse speed. From the measured results, the different V_T level is pronouncedly defined, indicating the ferroelectric domain switching can be reached under low-power operation. In Fig. 7, the repeatable V_T states of -4V, -4.5V and -5V under the 6V erase state confirms the feasibility of multi-level operation.

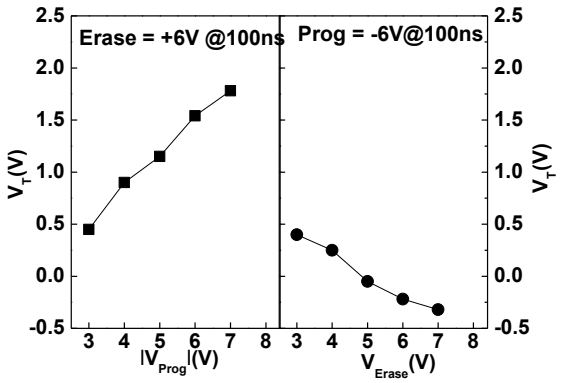

Fig. 6 V_T shift characteristic at various program/erase voltages

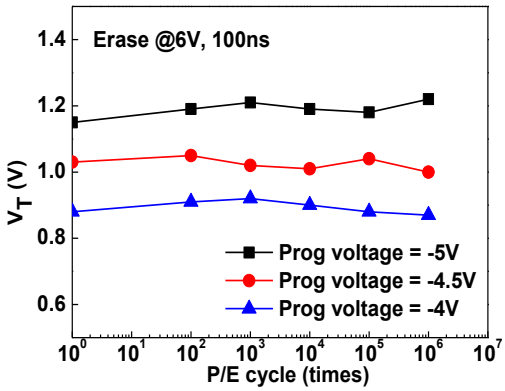

Fig. 7 Multi-level operation under 6V-100ns erase state

4. Conclusions

The simple design of 1T, fast 100-ns switching at low P/E voltages of 6V, and multi-level operation have been confirmed in this novel ferroelectric versatile memory.

Acknowledgements

This work was supported by the National Science Council (NSC) of Taiwan, Republic of China, under contract No. NSC 105-2221-E-003-022 and 105-2221-E-009-139-MY3.

References

[1] C. H. Cheng *et al.*, IEEE Electron Device Lett., **35** (2014) 138.

[2] Y. C. Chiu *et al.*, *Symp. on VLSI Technology* (2015) 184.

[3] Y. C. Chiu *et al.*, *International Reliability Physics Symposium* (2015) MY.3.1.

[4] Y. C. Chiu *et al.*, *Symp. on VLSI Technology* (2016) 150.

[5] Y. C. Chiu *et al.*, *International Reliability Physics Symposium* (2016) MY.7.x