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Effect of Interface Traps on the Device Performances of the Tunneling Field-Effect Transistors Based on InGaAs

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Abstract

In this work, the effect of interface traps on gate-all-around (GAA) tunneling field-effect transistors (TFETs) was investigated by TCAD. The interface trap was electrically energetic defects with energy distribution in the energy bandgap of semiconductor. The InGaAs-based TFETs are simulated to analyze the electrical contribution of interface traps in TFETs. The threshold voltage (V_{th}), on-state current (I_{on}), and off-state current (I_{off}) are extracted by simulations. The acceptor-like interface traps in TFETs based on InGaAs, which is the direct bandgap materials, had an influence on the on-state characteristics. On the other hand, the effect of interface traps in Si-TFETs was stronger on the off-state region.

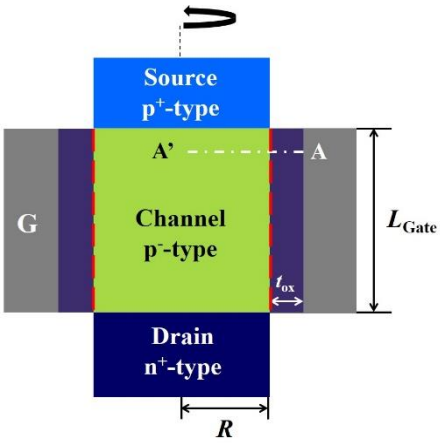
1. Introduction

The semiconductor devices based on metal-oxide-semiconductor structure have problems related to high trap density (N_{it}) at the gate dielectric/semiconductor interface. They result in high leakage current, low-frequency noise, and degradation of mobility and drain current. The interface traps occupied by electrons or holes contribute to threshold voltage (V_{th}) shifts and the increase of leakage current which give rise to large subthreshold swing (S) above 60 mV/dec due to interface trap [1]. Therefore, it is important that effect of interface traps on the compound semiconductor TFETs is analyzed and evaluated. The current drivability of TFETs is dominated by the band-to-band tunneling (BTBT) which is controlled by the tunneling barrier between the source region and the channel region. The energy band of channel region can be changed by the interface trap charges. Therefore, they result in a reduction of the tunneling rate with the increase of tunneling barrier width due to the acceptor-like traps [2].

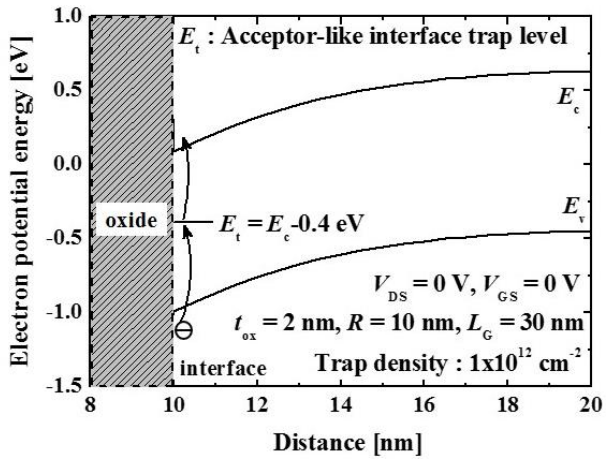
In this work, we analyze the impact of interface traps on gate-all-around (GAA) TFETs based on InGaAs layers by technology computer-aided designed (TCAD) simulation [3]. The correlation of the trap assistance tunneling (TAT) and the interface traps is investigated for TFETs and we could confirm that the leakage current increases by the interface trap and Shockley-Read-Hall (SRH) generation/recombination. Properties of the V_{th}, on-state current (I_{on}), and off-state current (I_{off}) in InGaAs-based TFETs are shown according to various acceptor-like interface traps with those of Si-based TFETs.

2. Simulation Results and Discussion

Device structure and interface trap characteristics



(a)



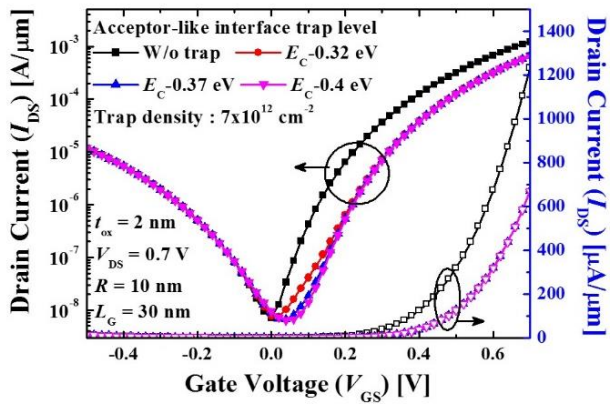
(b)

Fig. 1 (a) Symmetrical device structures of the InGaAs- and the Si-based GAA TFETs with interface trap (red dash line) (b) illustration of energy band diagram with TAT+SRH at oxide/Si interface as extracted following A-A' line in (a).

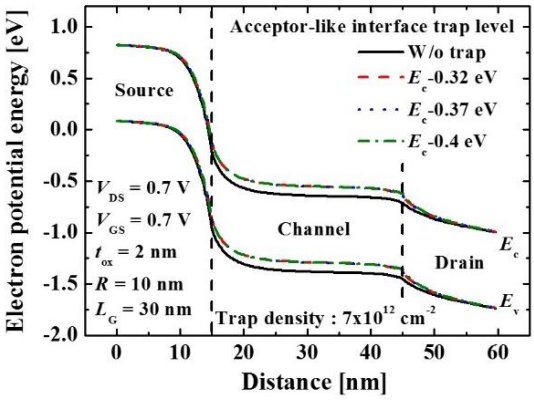
Fig. 1(a) shows the cross section of GAA TFETs with the gate length (L_G) of 30 nm, the radius (R) of 10 nm, and the gate oxide thickness (t_{ox}) of 2 nm. The doping concentrations of p^+-source, p^--channel, and n^+-drain are 5×10^{19} cm^{-3}, 1×10^{16} cm^{-3}, and 5×10^{18} cm^{-3}, respectively. The dash

line between the oxide and the semiconductor indicates the distribution interface traps. The 2-D simulations was performed with nonlocal BTBT model, SRH model, TAT model, and interface trap model. As shown in Fig. 1(b), the energy band diagram with accept-like trap level (E_t) is extracted following A-A' line in Fig. 1(a). The density of interface trap (N_{it}) is 1×10^{12} cm^{-2}. The interface traps result in the boosting of TAT. Interface TAT and SRH from the source region to the channel region through the interface region is able to increase the leakage current at an off-state [2].

DC characteristics



(a)



(b)

Fig. 2 (a) Transfer curves of InGaAs-based GAA TFETs, (b) energy band diagrams in InGaAs-based TFETs at on-states dependent on acceptor-like interface trap levels.

Fig. 2(a) shows the transfer curves of InGaAs-based GAA TFETs with respect to acceptor-like interface trap levels. Left and right axes indicate the logarithmic and linear scales, respectively. InGaAs is the direct bandgap material and a bandgap of InGaAs is 0.74 eV. Moreover, the electron effective mass of InGaAs is small compared with that of Si. An ambipolar effect of transfer characteristics with InGaAs-based TFETs remarkably occurs and I_{off}'s according to the trap levels are near contact. TFETs with interface traps have lower I_{on} compared with those without interface

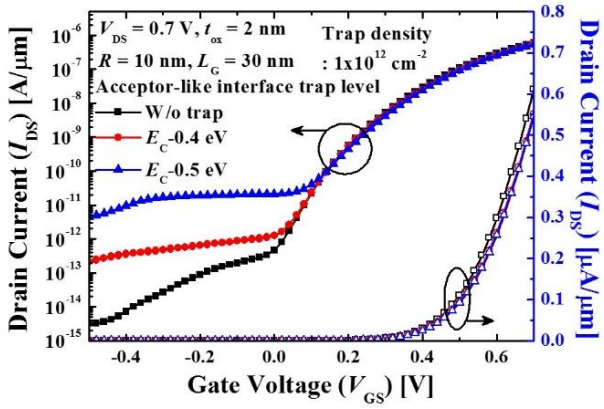


Fig. 3 I_{DS}-V_{GS} curves Si-based GAA TEFTs dependent on acceptor-like interface trap levels.

traps, since tunneling current from source to channel is reduced due to trapping of electrons by interface traps. As shown in Fig. 2(b), the electron potential band near the interface region is raised by interface trap charge. In the results, the tunneling current and the subthreshold slope reduces and it is a cause of V_{th} shift because of existing interface trap charge with accept-like interface trap. Fig. 3 shows the I_{DS}-V_{GS} curves of Si-based GAA TFETs with different acceptor-like interface trap levels. The leakage current with interface trap increases when the gate voltage (V_{GS}) is below 0 V. The I_{off} at E_t, which is almost middle level (E_c-0.5), rapidly rise. Si is the indirect bandgap semiconductor and the deep E_t in Si exists. The TAT and SRH by the interface traps and the deep traps in Si result in larger leakage current.

3. Conclusions

Tunneling current by BTBT mechanism between the source junction and the channel has been affected by the interface traps in MOS structure. Potential energy band of near the interface region has been raised by interface trap charges. The tunneling current of InGaAs TFETs has reduced due to charges existed in interface trap. In a case of Si-FET, however, TAT and SRH have increased I_{off}.

Acknowledgements

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