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# ZnO and ZnON Film-Profile Engineered TFTs for BEOL High-Voltage Operations

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**Abstract**

**In this work, we fabricated and characterized ZnO and ZnON TFTs with designed gate-to-drain offset lengths ($L_{GDO}$) in film-profile engineering (FPE) approach and evaluate their performance for BEOL high-voltage operation. An increase in $L_{GDO}$ increases the breakdown voltage ($V_{BD}$) at the expense of reduced transconductance ($g_m$). To sustain high $V_{BD}$ and $g_m$ of devices with a large $L_{GDO}$, the use of a ZnON channel is preferable. ZnON TFTs with high $V_{BD}$ of 70 V and $g_m$ of 13 μS is achievable with $L_{GDO}$ = 0.3 μm.**

## 1. Introduction

Recently Kaneko *et al*. proposed a novel InGaZnO (IGZO) TFT technology as the I/O voltage-bridging between CMOS LSIs and peripheral circuits/loads [1]-[2]. Very soon the oxide-semiconductor (OS) device technology has gained increasing attention for its easy integration to the BEOL of a chip thanks to the low-temperature fabrication processes. Since the peripheral circuits/loads usually operate at voltages much higher than the core CMOS circuitries, high-voltage (HV) OS TFTs are needed. In this regard, a structure equipped with a gate-to-drain offset (length = $L_{GDO}$) was realized in the devices to increase $V_{BD}$ [2]. In this work, we fabricated ZnO and ZnON devices with designed $L_{GDO}$ using a FPE method proposed previously [3], and study the impact of the $L_{GDO}$ on device characteristics.

## 2. Device fabrication

The fabrication process of FPE TFTs with gate-to-drain offset structure is illustrated in Fig. 1. A 100 nm-thick TiN layer was deposited over a nitride-capped Si substrate followed by a patterning step to form the TiN gate electrode. Next, a bi-layer deposition of a 400 nm-thick oxide and a 200 nm-thick TiN were conducted in sequence using PECVD and sputtering, respectively, to serve as the sacrificial oxide and hardmask (HM). Following the delineation of TiN HM and S/D regions as well as the removal of the sacrificial oxide, a nominally 40 nm-thick gate oxide and then a 50 nm-thick OS channel film (ZnO or ZnON) were deposited using PECVD and RF magnetron sputter, respectively. The device fabrication was completed by thermal evaporation of 120 nm-thick Al for S/D electrodes and a deposition of a PECVD TEOS oxide for the passivation layer. Finally, the test samples were annealed at 300°C for 30 mins in vacuum ambient.

## 3. Results and discussion

Figs. 2 (a) and (b) show the TEM micrographs of fabricated ZnO TFTs with $L_{GDO}$ = -0.3 μm (G/D-overlap) and $L_{GDO}$ = +0.3 μm (G/D-offset), respectively. It can be clearly seen that, owing to the shadowing effect of the suspended HM [3][4], the thicknesses of deposited channel and gate oxide film gradually decrease toward the center of the device. In the S/D regions of the G/D-offset device shown in Fig. 2(b) the stacked Al/ZnO/$SiO_2$ can be distinguished, while the gate electrode is offset from the edge of drain electrode with a distance of 0.3 μm, different from that of the G/D-overlap device (Fig. 2(a)). Figs. 3 and 4 show the transfer and output characteristics, respectively, of ZnO and ZnON TFTs with $L_{GDO}$ ranging from -0.3 to 0.3 μm. The insets in Fig. 3 show the drain currents of the TFTs under gate over-drive conditions. The reduction of the on-current with increasing $L_{GDO}$ is observed clearly, despite the fact that both $V_{TH}$ and subthreshold swing (SS) remain nearly unchanged. The output curves measured at $V_G$-$V_{TH}$ = 2 V for the devices also reveal a similar trend in Fig. 4. In Fig. 5, $V_{BD}$ of the ZnO and ZnON TFTs was obtained by measuring the gate leakage ($I_G$) as a function of drain voltage ($V_D$) when TFTs biased at off-state condition ($V_S$ = $V_G$ = 0V) based on the scheme proposed in [2]. Extracted $V_{BD}$ and $g_m$ as a function of $L_{GDO}$ for both ZnO and ZnON TFTs are plotted in Fig. 6. Increasing $L_{GDO}$ significantly increases $V_{BD}$ in company with a continuous reduction in $g_m$. The $g_m$ of ZnO TFT with large $L_{GDO}$ is less than 2 μS owing to the high resistance of the offset channel. In this study, we found that the dilemma can be relieved with the use of a ZnON channel, which has been demonstrated to exhibit much higher electron mobility than ZnO and IGZO [5]. Both high $V_{BD}$ (70 V) and $g_m$ (13 μS) of ZnON TFTs are achievable with $L_{GDO}$ = 0.3 μm although the $V_{BD}$ values for ZnON TFTs are slightly smaller than that of ZnO TFTs due to the reduced resistances of the offset channel [6]. The above improvement offered by the ZnON TFT can be attributed to the reduction of the resistance components ($R_{S/D}$ and $R_{ch}$), as shown in Fig. 7. Fig. 8 depicts the output characteristics for HV operation (maximum $V_D$ is 60 V) of a TFT with $L_{GDO}$ = 0.3 μm.

## 3. Conclusions

We have fabricated and characterized FPE TFTs with channel made of ZnO or ZnON and designed $L_{DGO}$ for HV operation. $V_{BD}$ increases with increasing $L_{DGO}$ at the expense of degraded $g_m$. ZnON TFTs are demonstrated to have a significant reduction in $R_{on}$ while maintain a high

$V_{BD}$ as compared with the ZnO counterpart. By taking the trade-offs between various parameters into account, the high-mobility ZnON channel appears to be a suitable material for high-performance HV OS TFTs.

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## References

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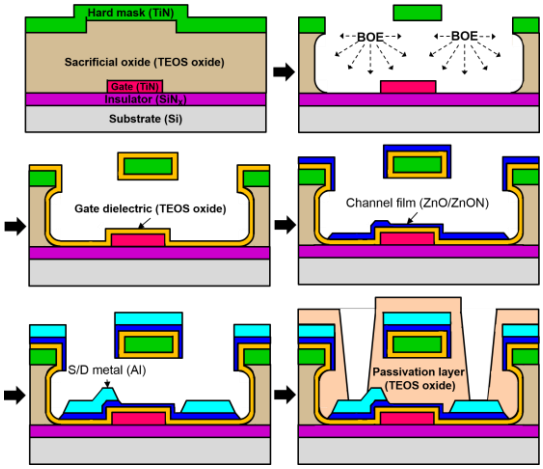


Fig. 1 Process flow for fabricating the FPE oxide-based TFTs with gate/drain-offset

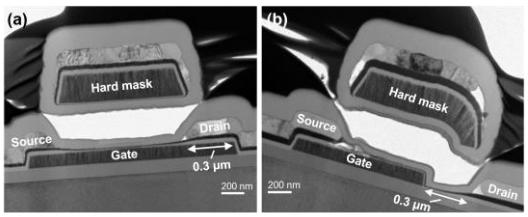


Fig. 2 Cross-sectional TEM images of ZnO TFTs with $L_{GDO}$ of (a) -0.3μm and (b) 0.3μm

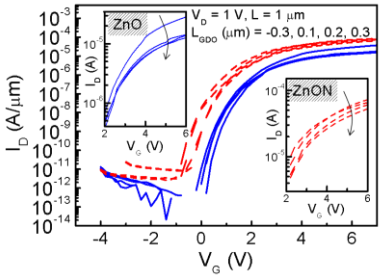


Fig. 3 Transfer characteristics of ZnO (solid lines) and ZnON (dashed lines) TFTs with different $L_{GDO}$.

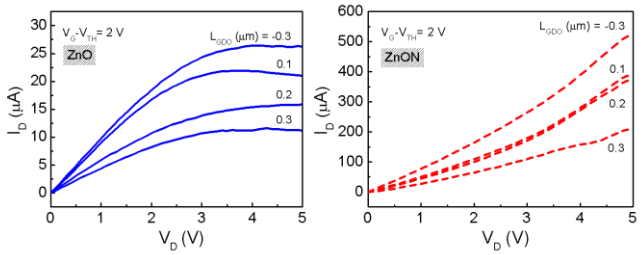


Fig. 4 (a) Output characteristics of ZnO and ZnON TFTs with different $L_{GDO}$.

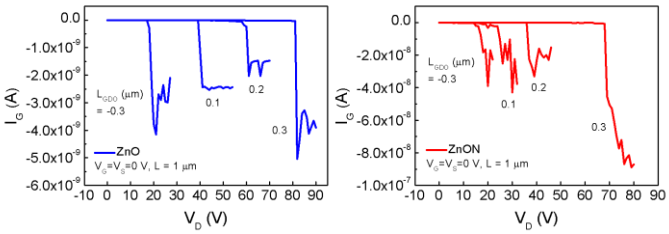


Fig. 5 $I_G$ as a function of $V_D$ measured under $V_S$=$V_G$=0 V for determination of $V_{BD}$ of the ZnO and ZnON TFTs.

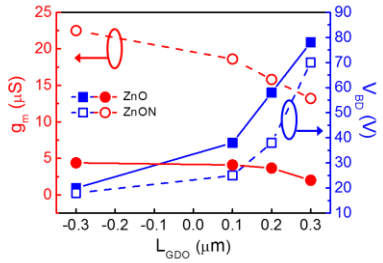


Fig. 6 The extracted $V_{BD}$ and $g_m$ of ZnO and ZnON TFT as a function of $L_{GDO}$.

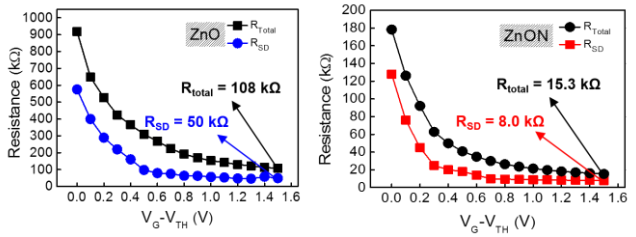


Fig. 7 The extracted channel resistance $R_{ch}$ (= $R_{total}$ - $R_{S/D}$) and source/drain resistance $R_{S/D}$ of ZnO and ZnON TFTs with $L_{GDO}$ of -0.3μm.

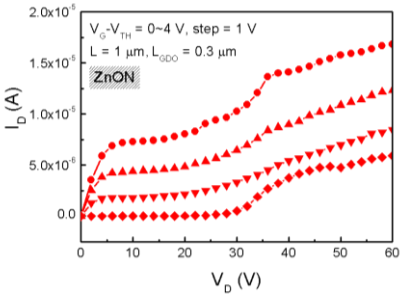


Fig. 8 Output characteristics of $V_D$ up to 60 V for a ZnON TFT with $L_{GDO}$ = 0.3 μm.