PS-6-12

Room-temperature Fabrication of Amorphous IGZO TFTs with Co-sputtered $Zr_xSi_{1-x}O_2$ Gate Dielectrics

Pang-Yi Liu[1], Shui-Jinn Wang*[1, 2], Chien-Hsiung Hung[1], Chien-Hung Wu[3], Nai-Sheng Wu[1], Hao-Ping Yan[1], and Tseng-Hsing Lin[1]

[1]Institute of Microelectronics, Dept. of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan.
[2]Advanced Optoelectronic Technology Center, National Cheng Kung University, Tainan, Taiwan
[3]Department of Electronics Engineering, Chung Hua University, Hsinchu, Taiwan.
*Phone: +886-6-2763882, E-mail: sjwang@mail.ncku.edu.tw

Abstract:

The use of co-sputtered zirconium silicon oxide ($Zr_xSi_{1-x}O_2$) gate dielectrics to improve gate controllability of amorphous indium gallium zinc oxide (α-IGZO) thin-film transistors (TFTs) is proposed and demonstrated. Through adjusting the sputtering power of the SiO_2 target with that of the ZrO_2 target kept at 100 W, a dielectric constant ranging from about 28.1 to 7.8 is obtained. Immunity of poly-structure formation of the $Zr_xSi_{1-x}O_2$ dielectrics at evaluated temperatures (600 °C) is also examined. Our experimental results reveal that the $Zr_{0.85}Si_{0.15}O_2$ gate dielectric prepared at a power ratio of ZrO_2:SiO_2=100 W:50 W could lead to a significantly improved device performance of subthreshold swing (103 mV/dec) and field effect mobility (33.76 $cm^2/V{\cdot}s$).

1. Introduction

In recent years, amorphous indium gallium zinc oxide (α-IGZO) thin-film transistor (TFT) has been widely used for flat-panel displays (FPDs) applications due to its wide band gap, high mobility, and high uniformity of device performance compared with conventional Si-based TFTs [1]. In order to strengthen field effect and reduce gate leakage current, attempts have been made to seek alternative high-κ dielectrics for α-IGZO TFTs [2]. Comparing with SiO_2 gate dielectric, nevertheless, high-κ materials usually have a larger amount of intrinsic defects which could degrade the device performances [3]. Zirconium dioxide (ZrO_2) is one of the most promising materials, it shows an excellent thermal stability especially when a suitable composition of silicon is incorporated. It is reported that Si ingredients could reduce the density of bulk defects and improve the quality of interface with IGZO channel layer [4]. In this study, effects of Si composition in the $Zr_xSi_{1-x}O_2$ dielectrics on the performance of α-IGZO TFTs are examined. The suitable RF power ratio for the co-sputtering of ZrO_2 and SiO_2 targets at room temperature to maximize the role of $Zr_xSi_{1-x}O_2$ dielectrics in α-IGZO TFTs is investigated. The hysteresis characteristics of the α-IGZO TFTs with $Zr_xSi_{1-x}O_2$ gate dielectrics are also discussed.

2. Experimental

An 8.5±0.5-nm-EOT $Zr_xSi_{1-x}O_2$ layer as gate dielectric was deposited on n^+-Si substrate by RF co-sputtering of ZrO_2 and SiO_2 targets in Ar ambient at room temperature. For the deposition of $Zr_xSi_{1-x}O_2$ dielectric, various sputtering power (0, 50, 100, and 150 W) were used for the SiO_2 target with the sputtering power for the ZrO_2 target was kept at 100 W. Subsequently, a 25-nm-thick α-IGZO channel layer was deposited using an IGZO target (In_2O_3:Ga_2O_3:ZnO=1:1:1) in Ar ambient by RF sputtering. Finally, a 25-nm-thick Al-doped ZnO (AZO) as a buffer layer and a 200-nm-thick Titanium (Ti) metal electrode as the source and drain (S/D) contact were deposited by RF sputtering and e-beam evaporation, respectively. The cross-sectional schematic of the α-IGZO TFTs with $Zr_xSi_{1-x}O_2$ gate dielectrics is shown in Fig. 1 with a width-to-length ratio of 200 μm/20 μm.

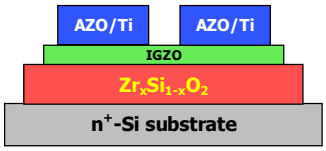

Fig. 1 Schematic of the α-IGZO TFTs with $Zr_xSi_{1-x}O_2$.

3. Results and Discussion

Based on X-ray photoelectron spectroscopy (XPS), C-V measurement, and spectroscopic ellipsometry (SE), the κ-value, the Si compositions, and the surface roughness in the $Zr_xSi_{1-x}O_2$ films prepared under different sputtering powers for SiO_2 were shown in Fig. 2 and Table I, respectively. The κ-value of $Zr_xSi_{1-x}O_2$ dielectrics are of 28.1, 26.5, 13.4, and 7.8 for the sample prepared with a co-sputtering power ratio (ZrO_2 (W):SiO_2 (W)) of 100:0 (ZrO_2), 100:50 ($Zr_{0.85}Si_{0.15}O_2$), 100:100 ($Zr_{0.45}Si_{0.55}O_2$), and 100:150 ($Zr_{0.2}Si_{0.8}O_2$), respectively. It indicates that the κ-value and Si/(Si+Zr) ratio could be adjusted by the co-sputtering power ratio. Our results indicate that the $Zr_{0.85}Si_{0.15}O_2$ film has the smoothest surface (roughness < 1 nm) as compared with the other samples. Accordingly, suppressed surface scattering and reduced interface trap density after the α-IGZO channel layer deposition can be expected. Note that the fabricated α-IGZO TFTs with the above mentioned four types of gate dielectric are referred as device A, B, C, and D, respectively.

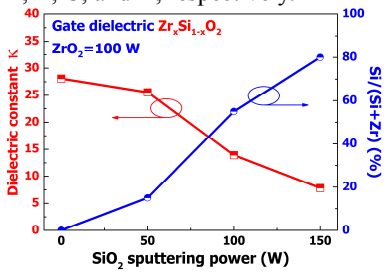

Fig. 2 Dielectric constant and Si/(Si+Zr) ratio of $Zr_xSi_{1-x}O_2$ film as a function of co-sputtering power ratio of ZrO_2 and SiO_2.

Table I Si ingredients and Dielectric constant of $Zr_xSi_{1-x}O_2$ films with different co-sputtering power ratios.

Power ratio: ZrO_2(W):SiO_2 (W)	Si/(Si+Zr) (%)	Dielectric	κ	Roughness (nm)
100:0	0	ZrO_2	28.1	5.27
100:50	15	$Zr_{0.85}Si_{0.15}O_2$	26.5	<1
100:100	55	$Zr_{0.45}Si_{0.55}O_2$	13.4	3.01
100:150	80	$Zr_{0.2}Si_{0.8}O_2$	7.8	4.79

Figure 3 shows the XRD analysis of ZrO_2 and $Zr_xSi_{1-x}O_2$ films without and with PDA for 10 min in O_2 at 600 °C.

It is seen that the as-deposited ZrO_2 layer has a polycrystalline structure. On the contrary, the $Zr_xSi_{1-x}O_2$ film remains amorphous state even after intentional post-deposition annealing (PDA) at 600 °C in O_2 ambient, which favors for leakage current reduction. Figure 4 shows the J-V curve of ZrO_2 and $Zr_xSi_{1-x}O_2$ films. With the incorporation of SiO_2, in addition to the stable amorphous structure, the band gap of $Zr_xSi_{1-x}O_2$ increases as increasing the SiO_2 sputtering power, as a result, the leakage current density is largely suppressed. These results suggest that the $Zr_xSi_{1-x}O_2$ film should be more appropriate for gate dielectric than ZrO_2 films.

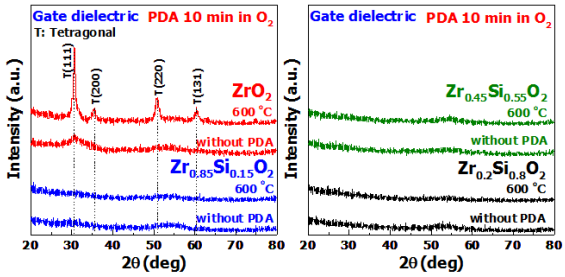

Fig. 3 The XRD analysis of ZrO_2 and $Zr_xSi_{1-x}O_2$ films without and with PDA for 10 min in O_2 at 600 °C.

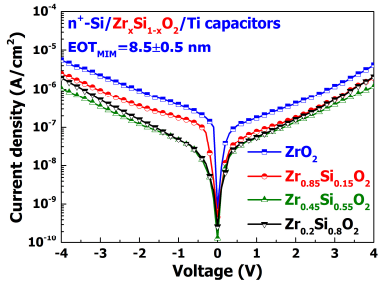

Fig. 4 The J-V characteristics of n^+-Si/$Zr_xSi_{1-x}O_2$/Ti capacitor structure.

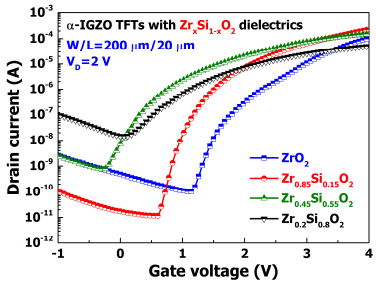

Fig. 5 The transfer characteristics of the α-IGZO TFTs with ZrO_2 and $Zr_xSi_{1-x}O_2$ gate dielectrics.

Figure 5 shows the transfer characteristics of the α-IGZO TFTs with ZrO_2 and $Zr_xSi_{1-x}O_2$ films. The extracted device electrical parameters are listed in Table II. It reveals that α-IGZO TFT with $Zr_{0.85}Si_{0.15}O_2$ (device B) shows the best electrical performance with highest I_{on}/I_{off} of 1.96×10^7, lowest subthreshold swing (SS) of 103 mV/dec, highest field-effect mobility (μ_{FE}) of 33.76 $cm^2/V\cdot s$, lowest D_{it} of 1.90×10^{12} $cm^{-2}eV^{-1}$, lowest hysteresis ΔV_{hys} of 0.30 V. It suggests that D_{it} at $Zr_xSi_{1-x}O_2$/IGZO interface can be effectively suppressed and the gate controllability is enhanced. Hence a lower SS, higher μ_{FE}, and higher I_{on}/I_{off} can be obtained from a suitable Si ingredient incorporation. However, the devices with $Zr_{0.45}Si_{0.55}O_2$ and $Zr_{0.2}Si_{0.8}O_2$ gate dielectrics show poor performance, probably due to excessive Si ingredients in $Zr_xSi_{1-x}O_2$ lead to rough surfaces and degrade the quality of the $Zr_xSi_{1-x}O_2$/IGZO interface.

Fig. 6 shows the hysteresis characteristics of the α-IGZO TFTs with ZrO_2 and $Zr_{0.85}Si_{0.15}O_2$ gate dielectrics. It indicates that Device B has the lowest ΔV_{hys} (0.30 V) among all prepared devices. It suggests that suppressed interface trap density and reduced gate leakage current can be achieved from the $Zr_xSi_{1-x}O_2$ dielectric film with a suitable co-sputtering ZrO_2 and SiO_2 [5].

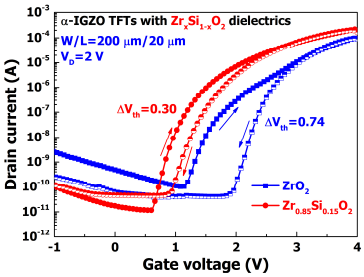

Fig. 6 The transfer characteristics of the α-IGZO TFTs with ZrO_2 and $Zr_{0.85}Si_{0.15}O_2$ gate dielectrics under the forward (V_{GS}=-1 to 4 V) and reverse (V_{GS}=4 to -1 V) sweeps.

Table II Comparisons of device parameters of α-IGZO TFTs with ZrO_2 and $Zr_xSi_{1-x}O_2$ gate dielectrics.

Device	I_{on}/I_{off}	V_{TH} (V)	SS (mV/dec)	μ_{FE} ($cm^2/V\cdot s$)	D_{it} ($cm^{-2}eV^{-1}$)	ΔV_{hys} (V)
A	1.03×10^6	1.49	141	27.69	3.32×10^{12}	0.74
B	$\mathbf{1.96\times10^7}$	**0.96**	**103**	**33.76**	$\mathbf{1.90\times10^{12}}$	**0.30**
C	2.00×10^5	2.40	213	16.61	6.50×10^{12}	0.42
D	3.54×10^3	--	424	2.81	1.54×10^{13}	-
[5]	7.50×10^5	4.26	310	4.3	7.00×10^{12}	1.78
[6]	1.20×10^6	-1.0	240	8.4	-	-

4. Conclusions

Improved performance of α-IGZO TFTs with $Zr_xSi_{1-x}O_2$ gate dielectrics have been successfully fabricated by co-sputtering of ZrO_2 and SiO_2 target at room temperature. The κ-value of $Zr_xSi_{1-x}O_2$ could be adjusted through the sputtering power ratio. In addition, the incorporation of Si in $Zr_xSi_{1-x}O_2$ film could avoid of poly-crystallization even after PDA at 600 °C. In addition, it is found that the $Zr_{0.85}Si_{0.15}O_2$ film prepared at a power ratio of ZrO_2:SiO_2=100 W:50 W has the lowest roughness, which could serve best as the gate dielectric to α-IGZO to suppress surface scattering and interface tap density. Our experiments show that the $Zr_{0.85}Si_{0.15}O_2$ gate dielectric could lead to a significantly improved device performance with reduced SS (103 mV/dec) and enhanced μ_{FE} (33.76 $cm^2/V\cdot s$).

Acknowledgements

This work was supported by the Ministry of Science and Technology (MOST), Taiwan, under contract No. MOST 104-2221-E-006-066 and MOST 104-2221-E-006130-MY3. The authors would like to thank the Advanced Optoelectronic Technology Center, National Cheng Kung University, Taiwan, for equipment access and technical support.

References

[1] J. S. Park *et al.*, Thin Solid Films. **520** (2012) 1679.
[2] Y. S. Chun *et al.*, Microelectron. Eng. **88** (2011) 1590.
[3] J. Robertson *et al.*, Mater. Sci. Eng. R. **88** (2015) 1.
[4] D. Cho *et al.*, Electron. Mater. Lett. **9** (2013) 381.
[5] L. X. Qian *et al.*, Microelectron. Rel. **54** (2014) 2396.
[6] F. H. Chen *et al.*, IEEE T. Dielect. El. In. **22** (2015) 3.