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Transport property of $NbSe_2/WSe_2$ van der Waals Junction

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Abstract

A transition metal dichalcogenide (TMD) $NbSe_2$ has recently received considerable attention due to its excellent metallic behavior even down to monolayer and significantly larger work function (~6 eV) among other TMDs. Therefore this material can be an efficient hole injecting electrode. Here, we show transport properties of $NbSe_2/WSe_2$ van der Waals (vdW) heterojunction fabricated by mechanical exfoliation and dry transfer. Two $NbSe_2$ flakes are transferred on WSe_2 flake to realize van der Waals contacts and the device is encapsulated by h-BN. The current transport measured between two $NbSe_2$ contacts through the WSe_2 channel exhibited p-type field effect transistor characteristics having small Schottky barrier height (~50 meV) at the vdW interface. The results suggest the vdW $NbSe_2$ contact is the excellent material to make p-type contact for TMDs. Adopting $NbSe_2$ as a contact material will give us the opportunity to explore a lot of unique characteristics specific to valence band transport such as valleytronics or vertical field effect transistors [1,2].

1. Introduction

Semiconducting TMDs such as MoS_2 and WSe_2 revealed unique layered crystal structure connected together by vdW inter-layer interaction. These crystals can be exfoliated down to monolayers and different layered crystals can be stacked together to build vdW heterostructures. The TMD-based vdW heterostructures have been drawn considerable attention owing to their potentially high performance for electronics and optoelectronics devices. Yet, the performances of these devices are occasionally limited by the large contact resistance between metal electrode and TMD. The preparation of highly transparent electrical contact to TMD has been extensively studied in last half decade. Most of previous studies used evaporation of metals on TMD to prepare the contacts, yet surface pinning or interface reaction at the metal/TMD interface are still serious issues. More recently, instead of the evaporated metal/TMD contact, the vdW contact between metallic layered material/TMD junctions are proposed to overcome the issues mentioned above [3]. Therefore, the detailed study on the transport property in such vdW junctions is highly demanded. $NbSe_2$ is known to be a metallic TMD and becomes superconducting at low temperature. Its work function of 6.0 eV is considerably higher than the valence band energy of semiconducting TMDs such as MoS_2 (5.6 eV) and WSe_2 (5.2 eV) [4]; therefore it is a great candidate to build a vdW contact for the purpose of hole injection. Here we fabricated $NbSe_2/WSe_2$ vdW junction and studied its transport properties.

2. Device fabrication procedure

Figure 1 shows the photograph and the schematic illustration of the fabricated device. By using mechanical exfoliation and PDMS-based transfer technique [5], stack of the layered materials are fabricated on the 300 nm SiO_2/Si substrate. Highly doped Si substrate works as a back gate electrode. First, hexagonal boron nitride (h-BN) with the thickness of ~30 nm is deposited on the substrate, followed by the transfer of few monolayer thick of WSe_2. Next, two $NbSe_2$ flakes are individually transferred to make contacts with WSe_2, and subsequently WSe_2 channel is capped by top h-BN flake with the thickness of ~30 nm. The width and length of the WSe_2 channel is 3.5 and 4 μm, respectively. Finally, electrical contacts to $NbSe_2$ are made with 40 nm Au/40 nm Ti fabricated by electron beam (EB) lithography and EB evaporation. All device fabrications are conducted at room temperature without introducing any heat treatment [6]. The device was loaded into the variable temperature cryostat, where the device was annealed at ~140 °C in He atmosphere for 6 hours prior to the electrical characterization.

3. Results

The back gate voltage V_{BG} dependence of the current I flow between the $NbSe_2$ contacts at different source-drain voltage V_{SD} at room temperature is presented in Fig. 2. This figure shows clear p-type field effect transistor characteristics. The current value in negative V_{BG} side (hole doped) is significantly larger than that of positive V_{BG} side (electron doped), suggesting that the $NbSe_2$ has much smaller potential barrier for hole injection than electron injection. We obtained current on-off ratio of 10^4 with on current value order of micro ampere at V_{SD} = 0.5 V. These properties are superior to that of $NbSe_2/W_xNb_{1-x}Se_2/WSe_2$ vdW contacts fabricated by CVD method [7]. We demonstrated high quality $NbSe_2/WSe_2$ vdW contact using exfoliation method.

The I-V_{SD} curves at V_{BG} = -50 V at room temperature (300 K) and 4 K are presented in Fig. 3 showing non-linear behavior. This suggests Schottky barrier formation at $NbSe_2/WSe_2$ interface. Fig. 4(a) presents temperature dependence of the drain current I at V_{SD} = 0.1 V. Arrhenius plot has been created from these curves, followed by the fitting according to the thermionic emission theory. The value of the barrier height was determined when the gate voltage dependence of the barrier height deviated from linear tendency as shown in Fig. 4(b). We obtained the Schottky barrier height at $NbSe_2/WSe_2$ interface of about 50 meV. The small Schottky barrier height suggests $NbSe_2$ works as a good hole injector to WSe_2.

4. Conclusion

In summary, we made $WSe_2/NbSe_2$ heterostructures encapsulated by h-BN by using mechanical exfoliation and PDMS dry transfer technique. The device showed the characteristics of a p-type field effect transistor, and the small barrier height was obtained by Arrhenius plot, inferring that vdW $NbSe_2$ contact could be a good p-type contact to WSe_2 and other TMDs.

Acknowledgements

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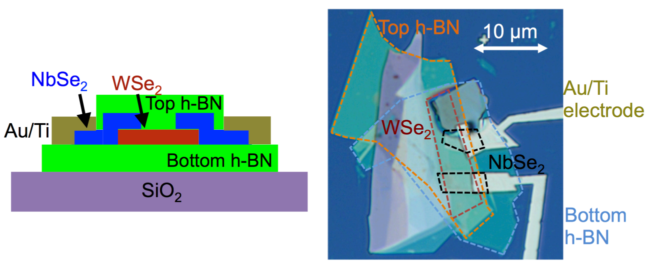

Fig. 1 (a) The device structure of $WSe_2/NbSe_2$ heterostructure encapsulated with h-BN. (b) Photograph of the device.

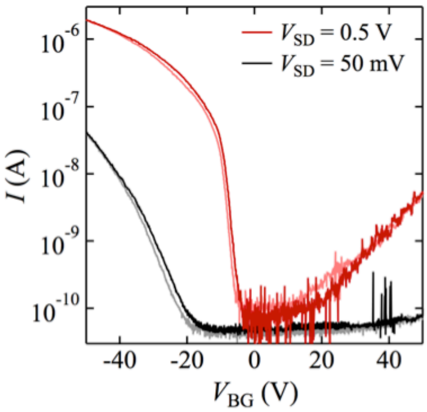

Fig. 2 V_{BG} dependence of the drain current I at different V_{SD} at room temperature.

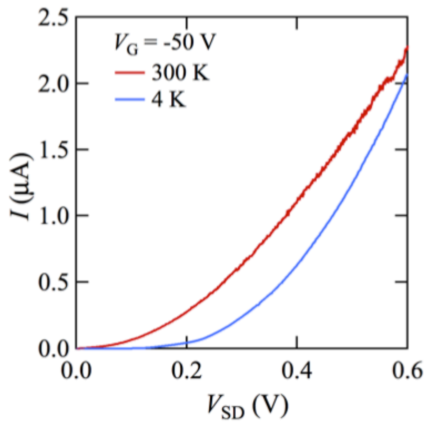

Fig. 3 I-V characteristics of the device measured at 300 K and 4 K at V_{BG} = -50 V.

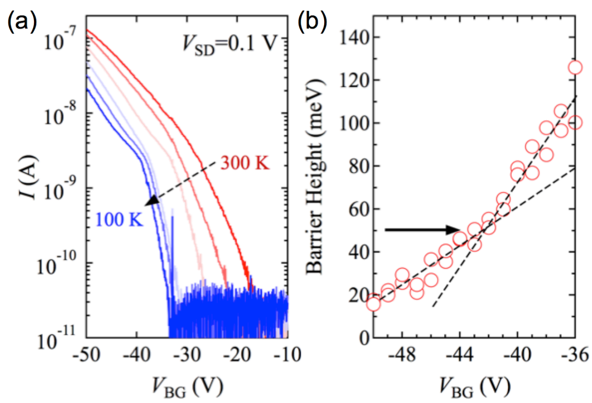

Fig. 4 (a) Temperature dependence of I-V_G characteristics of the device measured at V_{SD} = 0.1 V. (b) Gate voltage dependence of barrier height obtained from the fitting of Arrhenius plot.