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Gate-stack engineering of self-organized nanospherical Ge-gate/SiO_2/$Si_{1-x}Ge_x$-channel on Si (100) and Si (110) for Ge MOS devices

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Abstract

We report the first-of-its-kind, self-organized gate-stacking heterostructure of Ge-nanosphere (NP) /SiO_2 /SiGe-shell fabricated in a single step through selective oxidation of a SiGe nano-patterned pillar over buffer layers of Si_3N_4 on Si substrates. Process-controlled tunability of the Ge-NP size (10−120 nm), the SiO_2 thickness (2.5−5.0 nm), and as well the SiGe-shell thickness (2−22 nm) has been demonstrated over Si (100) or (110) substrates. Detailed morphologies and structural properties of the Ge-NP/SiO_2/SiGe-shell stacking structures were assessed. Single-crystalline $Si_{1-x}Ge_x$ shells with a Ge content as high as (x = 0.85) in a compressive stress state of 2.2% are achievable in our self-aligned gate-stack heterostructure, enabling a practically-achievable core building block for Ge-based MOS nano-electronic and photonic applications.

1. Introduction

Relentless miniaturization of feature sizes for CMOS devices has been widely pursued in order to boost IC performance. Aggressive downscaling into nanometer scale, however, is of formidable showstoppers not only for the process complexity and nonuniformity but also due to fundamental quantum limitation. In line with the development of exquisite process technology for continuing the downscaling track, the exploration of new materials, novel device structures, and innovative device architectures by leveraging on the wealth of CMOS technology know-how and infrastructures are highly desirable.

The inclusion of thin, strained layers of $Si_{1-x}Ge_x$ or Ge into Si CMOS technology is one of preeminent approaches to boost the performance of both MOSFETs and MOS-photonics built on the Si platform. Recently, we have demonstrated a unique gate-stacking structure for Ge MOS devices consisting of a self-organized SiO_2/Ge-NP/SiO_2/SiGe-shell over the Si(100) substrate [1]. Our approach is primarily based on the exquisite control available through lithographic patterning combined with the selective oxidation of $Si_{1-x}Ge_x$ nano-pillars over buffer layers of Si_3N_4 deposited over the Si substrates. Remarkably our MOS gate-stack structure is generated in a single-step process, effectively eliminating complicated microfabrication processes such as surface treatments and cleaning prior to the deposition of dielectrics onto the Ge. The good crystallinity of the Ge NPs is corroborated by the clear lattice fringes and sharp diffraction spots from HRTEM and selected-area diffraction (SAD) observations. Importantly, our MOS gate stack possesses good tunability for the Ge-NP size, the interfacial SiO_2 thickness, and the SiGe-shell thickness, thus providing a core building block for practical Ge-based MOS devices. Thereby, we have further advanced this unique heterostructure for the production of Al/SiO_2/Ge-NP/SiO_2/SiGe nanocrystal transistors with good charge retention and endurance [1] as well as for the fabrication of ITO/SiO_2/Ge-NP/SiO_2/SiGe phototransistors with superior photoresponsivity and very low dark current [2].

In this paper, we further advanced the controllability over the chemical composition and strain states of the SiGe-shells over SOI (100) and (110) substrates in order to further exploit high-performance Ge MOS nanoelectronics and nanophotonics.

2. Experimental results and discussion

Process flow and the corresponding transmission electron microscopy (TEM)/energy-dispersive x-ray spectroscopy (EDX) micrographs of Ge-NP/SiO_2/SiGe-shell over Si substrates are summarized in Fig. 1. Both thicknesses of the interfacial SiO_2 layer and the $Si_{1-x}Ge_x$ shell appear to increase with the Ge NPs penetrating deeper into the Si substrates when increasing oxidation time, and such a dependence is greatly enhanced when the crystal orientation of the Si substrates is changed from (100) to (110) (Fig. 2). As elaborated in our previous reports [4], the formation of the interfacial SiO_2 layer is an exquisitely-controlled dynamic equilibrium that exists between the concentration of Si interstitials emitted from Si substrates and external oxygen flux. The higher oxidation rate on the Si (110) crystal plane is because there are a higher number of surface atoms/chemical bonds than the (100) plane (available bonds: 9.59×10^{14} cm^{-2} for Si(110) versus 6.77×10^{14} cm^{-2} for Si(100)).

The formation of a thin, cup-shaped $Si_{1-x}Ge_x$ shell that is conformal with the Ge NP and the Si substrate is attributable to the Ge atoms migrating from the Ge NP and dissolving within the Si substrate. Figure 3(a) shows the Raman spectra for the variable-sized $Si_{1-x}Ge_x$ shells over Si(110). Considerable redshifts for both the longitudinal optical (LO) Ge-Ge phonon lines (295－300cm^{-1}) and the Si-Si lines (505－510cm^{-1}) were measured on the 50－120nm-long SiGe shells compared to the Raman lines of 301.5cm^{-1} for bulk Ge and 520cm^{-1} for bulk Si, respectively. We are able to extract the Ge content and strain states for each $Si_{1-x}Ge_x$ shell from the corresponding Raman shifts. A higher Si interstitial flux released from (110) Si crystal plane in combination with a lower diffusion coefficient for Ge within (110) Si crystal planes lead to the resulting $Si_{1-x}Ge_x$ shells over (110) Si surface having a lower Ge content of x = 0.3－0.35 in comparison to the $Si_{1-x}Ge_x$ shell with higher Ge content of x = 0.6－0.85 over Si(100) (Figure 3(b)). A lattice-constant mismatch between Ge and Si also leads to a compressive strain of -1.5% and -2.5% for

the $Si_{0.7}Ge_{0.3}$ shells over (110) Si and the $Si_{0.15}Ge_{0.85}$ shells over (100) Si, respectively. The large compressive strain states for the SiGe shells over Si(100) and over Si(110) are further experimentally evidenced by the top-view SAD examinations as shown in Figure 4.

3. Conclusion

We report the fabrication of self-organized gate-stacking heterostructure of Ge-nanosphere (NP)/SiO_2/SiGe-shell over Si(100) and Si(110) substrates. Good tunability of the geometrical conditions for the Ge-NP size (10−120 nm), the SiO_2 thickness (2.5−5.0 nm), and the SiGe-shell thickness (2−22 nm) has been demonstrated over Si (100) or (110) substrates. Ge contents of x = 0.6−0.85 with a compressive strain of -2.5% and x = 0.3−0.35 with a strain of -1.5% for the resulting $Si_{1-x}Ge_x$ shells over the Si(100) and over the Si(110), respectively, were extracted from the red shifts in Ge-Ge and Si-Si phone lines. This indicates that our self-aligned gate-stack heterostructure, enabling a practically-achievable core building block for Ge-based MOS nanoelectronic and photonic applications.

4. References

[1] W. T. Lai et al., Nanoscale Res. Lett., 10, 224, 2015.
[2] M. H. Kuo et al., Optics Lett., 40, 2401, 2015.

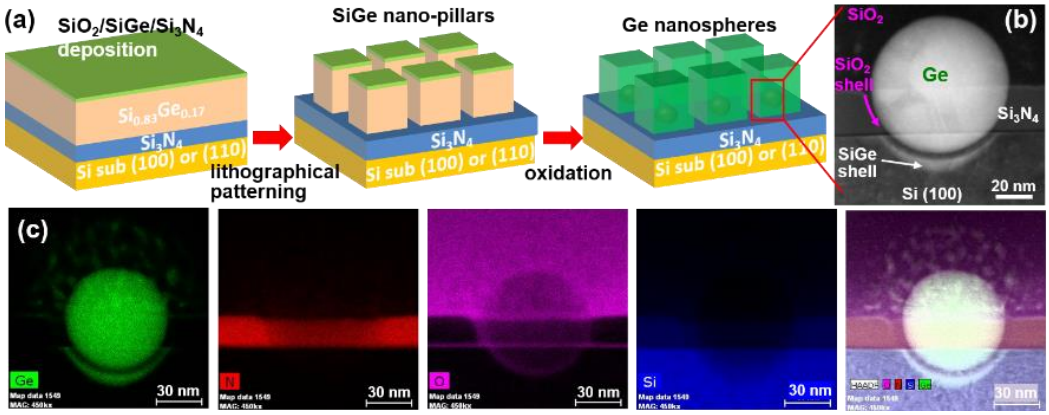


Fig. 1 Heterostructure of Ge NP/SiO_2/SiGe shell produced by thermally oxidizing SiGe nanopillar over buffer layers of Si_3N_4 on Si(100) substrate at 900°C for 25 min. followed by annealing at 875°C, 5minin an H_2O ambient. (a) schematics of experimental fabrication procedure, (b) STEM and (c) EDX mapping micrographs.

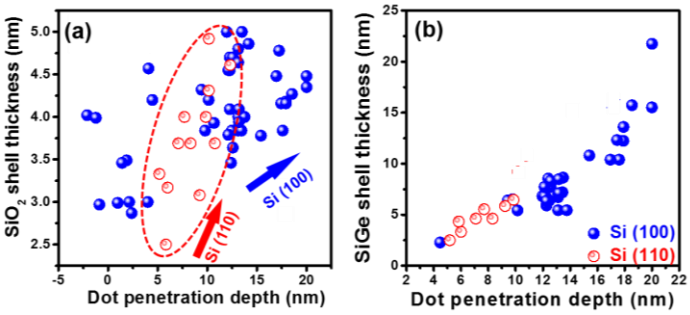


Figure 2 Thicknesses of (a) SiO_2 shell and (b) SiGe shell for the heterostructure of Ge dot/SiO_2/SiGe shell formed following 900°C in an H_2O ambient.

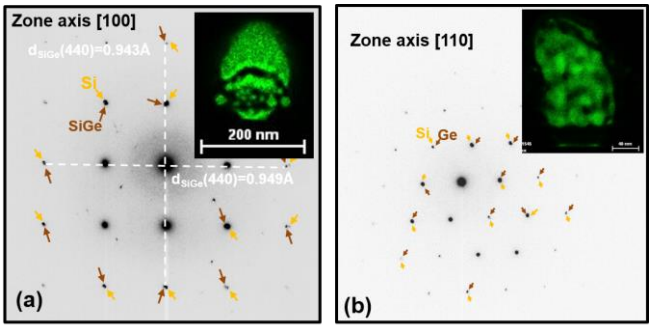
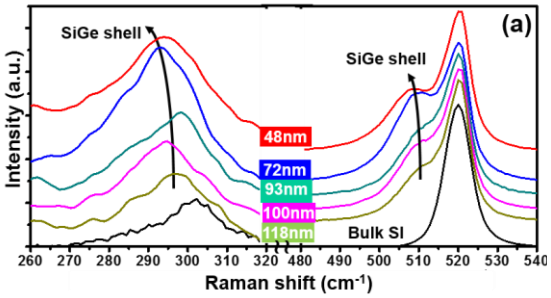


Figure 4 Top-view SAD for the SiGe shells over (a) SOI (100) and (b) SOI (110) substrates.



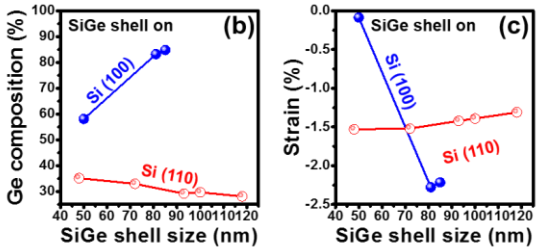


Figure 3 (a) Raman spectra for SiGe shell on SOI (110), (b) extracted Ge composition and (c) compressive strain for the SiGe shells over SOI (100) and SOI (110) substrates.