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Cross Point Type 1T-1MTJ STT-MRAM Cell with 60 nm Multi-pillar Vertical Body Channel MOSFET under 55 nm p-MTJ and Its Beyond for High Density STT-MRAM

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Abstract: In this paper, from the view point of cell size under keeping high speed writing of 10 nsec and DRAM compatible Vdd of 1.2V, the impact of novel cross point type 1T-1MTJ STT-MRAM cell with multi-pillar Vertical Body Channel (BC) MOSFET is shown for high density STT-MRAM. For that purpose, all combinations of MOSFET type and MTJ type are compared under the conditions that the channel length and channel width of 60 nm multi-pillar Vertical BC MOSFET are same as one of 90 nm planar MOSFET and MTJ's diameter (D_{MTJ}) is scaled down from 55 nm to 15 nm.

From the results, in all combination cases, it is made clear that with proposed cross point type 1T-1MTJ STT-MRAM cell with multi-pillar Vertical BC MOSFET, the cell size can be drastically suppressed by over 72% (in the best case: 88.5%) compared with conventional planar MOSFET type cell. Moreover, it is found that with the proposed cross point type cell technology, back bias effect at writing operation as one of issue of STT-MRAM can be overcame.

1. Introduction

A 1T-1MTJ STT-MRAM cell has a great potential to realize a high density STT-MRAM. In the case of conventional planar MOSFET based 1T-1MTJ STT-MRAM cell, it is reported that there are the best combinations of a MOSFET type (nMOSFET or pMOSFET) and a MTJ type (Bottom Pin; BP or Top Pin; TP) because of its back bias effect at writing operation [1, 2] as shown in Fig. 1. The BP indicates the pin layer is connected to the MOSFET and the TP indicates the pin layer is connected to Bit Line (BL).

In conventional planar MOSFET based 1T-1MTJ cell, the cell size was an issue due to BL and source line (SL) must be arranged in lateral as shown in Fig. 2. For achieving smaller cell size, many kinds of technologies were proposed. Especially, it was proposed that cross point type 1T-1MTJ STT-MRAM cell with “single pillar” Vertical BC MOSFET [3, 4] whose merits of the back bias effect free characteristics and excellent drivability are experimentally demonstrated [5]. However, “multi-pillar” Vertical BC MOSFET based cross point type 1T-1MTJ cell and its combinations of MOSFET type and MTJ type have not been discussed yet.

In this paper, the cell size of the cross point type 1T-1MTJ STT-MRAM cell with 60 nm multi-pillar Vertical BC MOSFET is evaluated under keeping high speed writing of 10 nsec and DRAM compatible Vdd of 1.2 V.

2. Proposed 1T-1MTJ Cell Structure

Fig. 3 shows the schematic diagrams of the 1T-1MTJ STT-MRAM cell with single pillar / multi-pillar Vertical BC MOSFET, respectively. 1T-1MTJ cell with single pillar and multi-pillar Vertical BC MOSFET have a cross point type cell structure.

3. Results and Discussion

The write operation performances of each type of 1T-1MTJ STT-MRAM cell are evaluated by HSPICE. The MTJ model and planar / Vertical BC MOSFET model of HSPICE are experimentally extracted as shown in Table I. To compare the performance of 1T-1MTJ cell with 60 nm Vertical BC MOSFET and that with 90 nm planar MOSFET, parameters such as L_g, V_{th}, and $R_{S/D}$ are made the equivalent.

Fig. 4 shows the write operation waveforms of 1T-1MTJ STT-MRAM cell with both planar MOSFET and multi-pillar Vertical BC MOSFET when MTJ switch from Parallel (P) to Anti-Parallel (AP). From these waveforms, for all combinations of MOSFET type and MTJ type, required channel width with keeping writing speed of 10 nsec under Vdd of 1.2 V are estimated. In Fig. 5, these required channel width are shown as a function of D_{MTJ} in the each MTJ switching (P -> AP, AP -> P). From the results, for all combination cases, it is shown that cross point type 1T-1MTJ STT-MRAM cell with multi-pillar Vertical BC MOSFET can achieve high speed writing of 10 nsec under Vdd of 1.2 V with extremely narrow channel width due to its excellent drivability and back bias effect free characteristics in comparison with conventional planar MOSFET type cell.

Cell size of each type 1T-1MTJ STT-MRAM cell is estimated from the above required channel width with following standard layout design rule [6] of STT-MRAM cell. In Fig. 6, the estimated cell size of each type cell is shown as a function of D_{MTJ}. It is shown that the cell size of the proposed cross point type 1T-1MTJ cell with multi-pillar Vertical BC MOSFET is suppressed over 72% (in the best case: 88.5%) compared with conventional planar MOSFET type cell. Moreover, Fig. 7 shows the cell size of cross point type 1T-1MTJ cell with multi-pillar Vertical BC MOSFET for all combinations of MOSFET type and MTJ type. It is found that with proposed cross point type cell, smallest cell size can be achieved by the combination of nMOSFET with better drivability and BP MTJ with better manufacturability in the case of MTJ size of less than 25 nm, even though in the previous reports with planar MOSFET type cell, pMOSFET or TP MTJ is required.

4. Conclusions

In this paper, it is made clear that under keeping high speed writing of 10 nsec and DRAM compatible Vdd of 1.2 V, proposed cross point type 1T-1MTJ STT-MRAM cell with multi-pillar Vertical Body Channel (BC) MOSFET is one of promising way for future high performance and high density STT-MRAM because it overcomes back bias effect.

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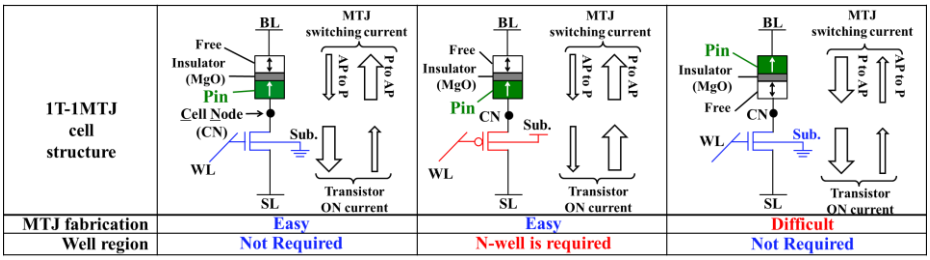

Fig. 1 Combinations of MOSFET type and MTJ type of 1T-1MTJ STT-MRAM cell.

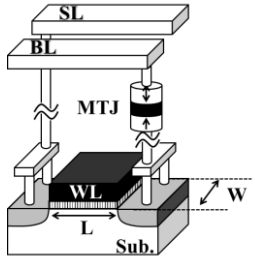

Fig. 2 Schematic diagram of planar MOSFET based 1T-1MTJ STT-MRAM cell.

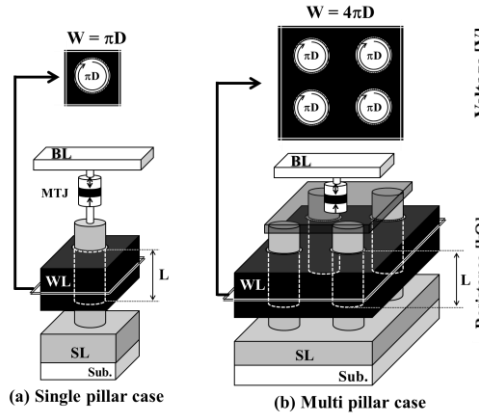

Fig. 3 Schematic diagram of cross point type Vertical BC MOSFET based 1T-1MTJ STT-MRAM cell.

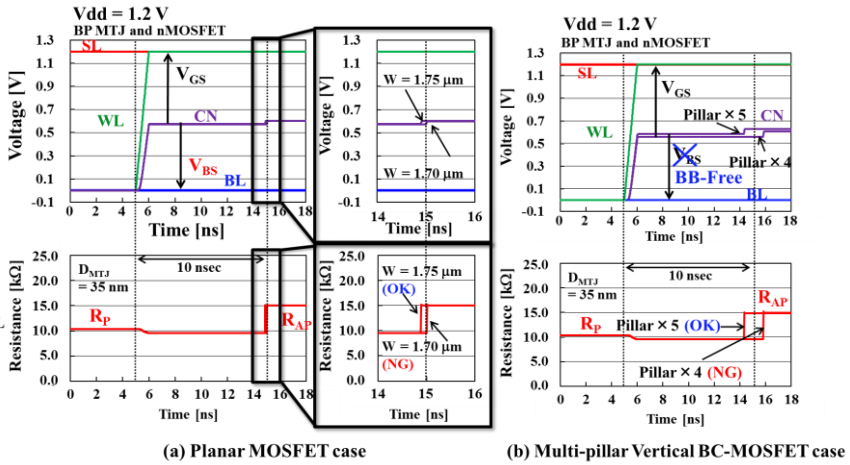

Fig. 4 Write operation waveforms of 1T-1MTJ STT-MRAM cell with both planar MOSFET and multi-pillar Vertical BC MOSFET when MTJ switch from Parallel (P) to Anti-Parallel (AP).

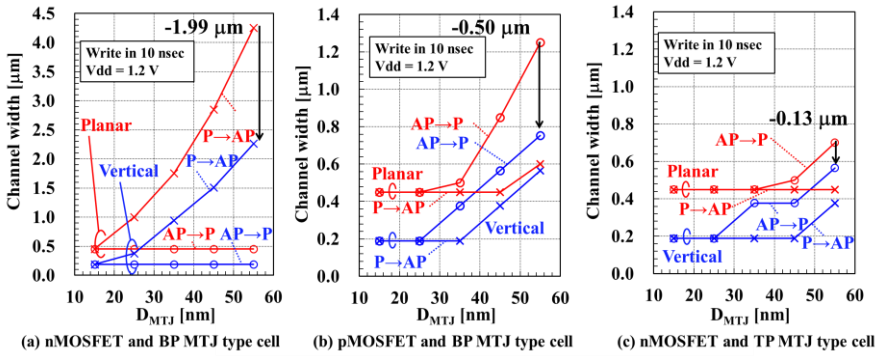

Fig. 5 Required transistor channel width as a function of D_{MTJ} in the each MTJ switching (P -> AP, AP -> P)

Table I Device parameters which are experimentally extracted.

Vertical BC MOSFET	
D_{pillar} [nm]	60
L_{gate} [nm]	100
Planar MOSFET	
L_{gate} [nm]	100
MTJ	
RA [Ω・μm²]	10
TMR [%]	100
$J_{AP\rightarrow P}$ [MA/cm²]	2.66
$J_{P\rightarrow AP}$ [MA/cm²]	5.34

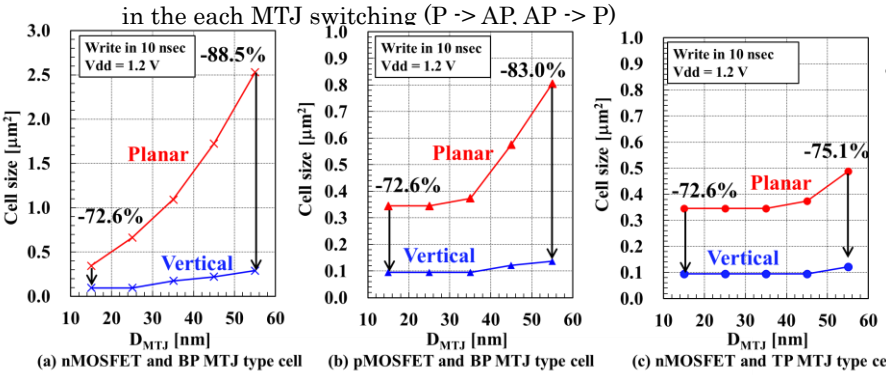

Fig. 6 Cell size dependency of each type 1T-1MTJ STT-MRAM cell on D_{MTJ}; planar MOSFET type vs. multi-pillar Vertical MOSFET type.

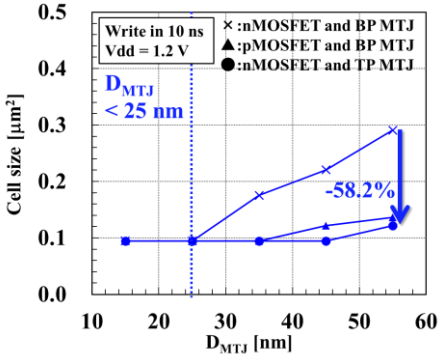

Fig. 7 Cell size of cross point type 1T-1MTJ cell with multi-pillar Vertical BC MOSFET for all combinations of MOSFET type and MTJ type.