Extended Abstracts of the 2017 International Conference on Solid State Devices and Materials, Sendai, 2017, pp37-38

A-6-02

Sub 1 V 60 nm Vertical Body Channel MOSFET Based 6T SRAM Array with Wide Noise Margin and Excellent Power Delay Product

Ryosuke Ogasawara[1,3,4], and Tetsuo Endoh[1,2,3,4]
[1]Graduate School of Engineering, Tohoku Univ. Japan, [2]Center for Innovative Integrated Electronic Systems, [3]JST-ACCEL, [4]JST-OPERA
Phone: +81-22-795-4906 E-mail: tetsuo.endoh@cies.tohoku.ac.jp

Abstract

In this paper, it is shown that 60 nm Vertical Body Channel (BC) MOSFET based 6T SRAM array achieves 0.84 V operation under the best Power Delay Product (PDP). Moreover, its PDP is improved by 31% in comparison with the 6T SRAM array based on 90 nm planar MOSFET which has the same channel length and channel width as those of the 60 nm Vertical BC-MOSFET. Additionally, 60 nm Vertical BC-MOSFET based 6T SRAM array achieves the improvement of 8.8% Read Static Noise Margin (RSNM), 16% Write Margin (WM).

1. Introduction

As scale down, smaller cell size, lower power, higher speed and wider noise margin are required for SRAMs as embedded cache memory of many kinds of logic chips. Therefore, advanced technologies of SRAM are extensively studied, e.g. new SRAM cell structure [1] , new SRAM array architecture [2], applied 3D structured MOSFET such as FinFET [3], Tri-Gate [4] and nanowire MOSFET [5]. Especially, it has been shown that SRAM cell size can be reduced by 180 nm Vertical MOSFET [6,7], as follows; the cell size of the 6T SRAM is reduced by 34% with the Vertical MOSFET compared with the planar MOSFET [7]. Moreover, it has various merits such as the reduction of transistor area, free from the back bias effect, the excellent drivability and off-leakage current. However, the Vertical BC-MOSFET based SRAM cell array performance such as noise margin, power delay product and its supply voltage dependency are not clear yet.

In this paper, by using 60 nm Vertical BC-MOSFET, SRAM cell array performance is evaluated for the first time.

2. Array Structure and Evaluation Methods

The structure of the Vertical BC-MOSFET [8,9] is shown in Fig. 1. Fig. 2 (a) shows the circuit diagram of 6T SRAM cell and Fig. 2 (b) shows the schematic diagram of 6T SRAM 256 bit cell array to evaluate read/write time. The source/drain resistance, V_{th} and EOT of the Vertical BC-MOSFET and the planar MOSFET are set equivalent. The W/L of every transistor is 0.19/0.10 μm in this study. The SRAM cell stability during hold and read operation are defined by SNM and RSNM. Write-ability is defined by WM, which is the maximum voltage on the bit-line needed to flip the cell content [10]. Read time is defined as the time from the point when WL reaches VDD/2 to the point when the voltage difference between bit-lines reaches 10% of VDD and write time is defined as the time from the point when WL reaches VDD/2 to the point when the voltage node Q reaches VDD/2 in this paper as shown in Fig. 3. The capacitance of bit-lines (CBL) is 0.5 pF in this study. All transistor models of 60 nm Vertical BC-MOSFET and 90nm planar MOSFET are experimentally extracted.

3. Results and Discussion

The Voltage Transfer Curves (VTCs) of the selected 6T SRAM cell with the Vertical BC-MOSFET and that with the planar MOSFET simulated by HSPICE are shown in Fig. 4. It is noted that the Vertical BC-MOSFET makes SNM and RSNM wider due to its steeper VTCs than the planar MOSFET. Owing to its high drivability and back bias free characteristic, the Vertical BC-MOSFET provides 8.8% wider RSNM and 16% wider WM of the selected 6T SRAM cell compared with the planar MOSFET at VDD=1.00 V as shown in Fig. 5 (a) and (b). Furthermore, the Vertical BC-MOSFET based 6T SRAM cell array can decrease VDD by 0.14 V and 0.09 V while keeping wider RSNM and WM than the planar MOSFET based 6T SRAM cell array, respectively. Fig. 6 shows the leakage in a 6T SRAM cell under various VDD. Because of its excellent off-leakage current characteristic, the Vertical BC-MOSFET can reduce the leakage by about 90% in a cell for various supply voltages.

Fig. 7 (a) and (b) show the simulated read time and write time of 6T SRAM cell array. Because of back bias free characteristic and high drivability of the Vertical BC-MOSFET, the Vertical BC-MOSFET based 6T SRAM cell array achieves about 10% shorter read time and about 20% shorter write time than the planar MOSFET based 6T SRAM cell array for each VDD (0.70 V ~ 1.00 V). Fig. 8 illustrates normalized power vs. speed during write operation. The Vertical BC-MOSFET based 6T SRAM cell array can achieve 30% higher speed with the same power or 30% lower power with the same speed during write operation. Fig. 9 shows normalized PDP of the 6T SRAM cell array during write operation vs. supply voltage. The Vertical BC-MOSFET provides 18% ~ 31% reduction of PDP and reduces the optimum supply voltage (V_{opt}) from 0.91 V to 0.84 V in 6T SRAM cell array compared with the planar MOSFET. The performance of the Vertical BC-MOSFET based 6T SRAM cell array and the planar MOSFET based 6T SRAM cell array are summarized in Table I. It is noted that the Vertical BC-MOSFET based 6T SRAM array is superior to the planar MOSFET based 6T SRAM array in all evaluation indices.

4. Conclusions

The performance of 60 nm Vertical BC-MOSFET based 6T SRAM cell array is evaluated for the first time. The supply voltage under the best PDP is suppressed from 0.91 V to 0.84 V by using 60 nm Vertical BC-MOSFET compared with 90 nm planar MOSFET which has the same W/L as the Vertical BC-MOSFET. Furthermore, it achieves 30% higher speed gain or 30% lower power during write operation. Additionally, the Vertical BC-MOSFET based 6T SRAM cell array has 8.8% wider RSNM and 16% wider WM at VDD=1.00 V in the selected cell. Moreover, the Vertical BC-MOSFET reduces leakage in a cell by about 90% under various supply voltages (0.70 V ~1.00 V). From the above,

Vertical BC-MOSFET based SRAM technology is one of the promising ways of low power, high speed and wide noise margin embedded cache memories for future MPU, MCU, GPU, etc.

Acknowledgements: This work was supported by JST-ACCEL Grant Number JPMJAC1301, JST-OPERA, and VDEC: The University of Tokyo with the collaboration with Synopsys Corporation.

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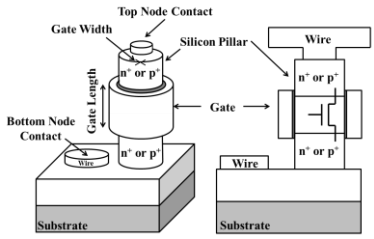
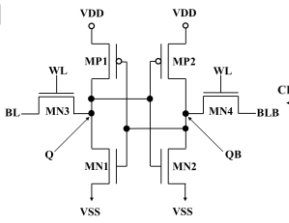


Fig. 1 Bird's view and cross-sectional view of the Vertical BC-MOSFET.



(a) (b)

Fig. 2 (a) Circuit diagram for 6T SRAM cell (b) Schematic diagram of the SRAM array for the read time and write time evaluations.

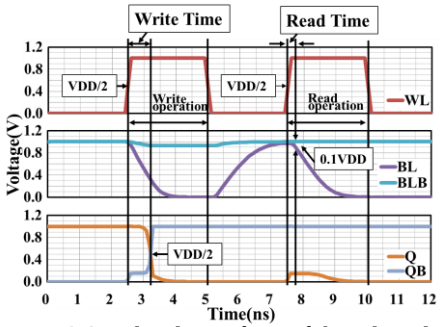
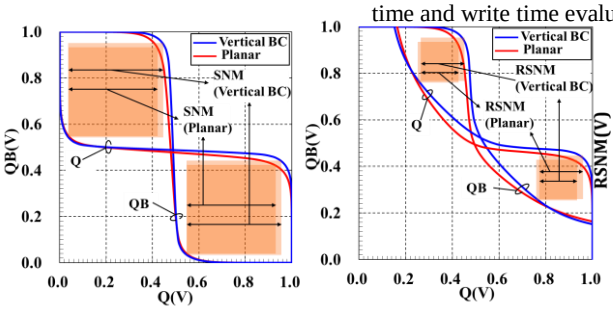
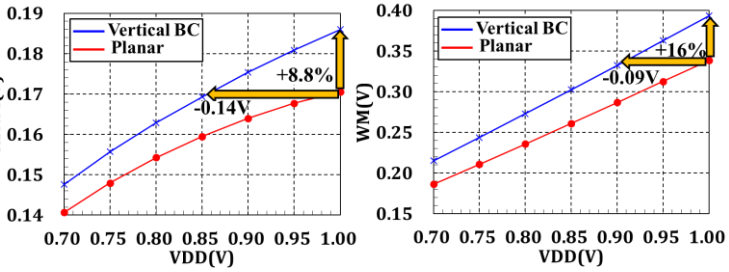


Fig. 3 Simulated waveform of the selected cell during read and write operation.



(a) Hold operation (b) Read operation

Fig. 4 Simulated VTCs (Voltage Transfer Curves) of the selected 6T SRAM cell with the Vertical BC-MOSFET and the planar MOSFET.



(a) (b)

Fig. 5 Simulated (a) RSNM and (b) WM of the selected 6T SRAM cell with the Vertical BC-MOSFET and the planar MOSFET.

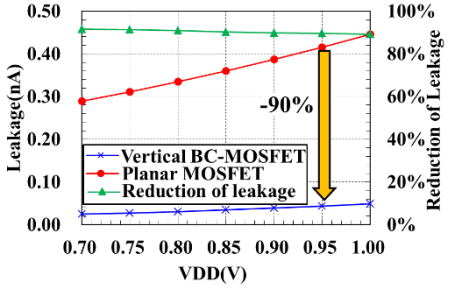
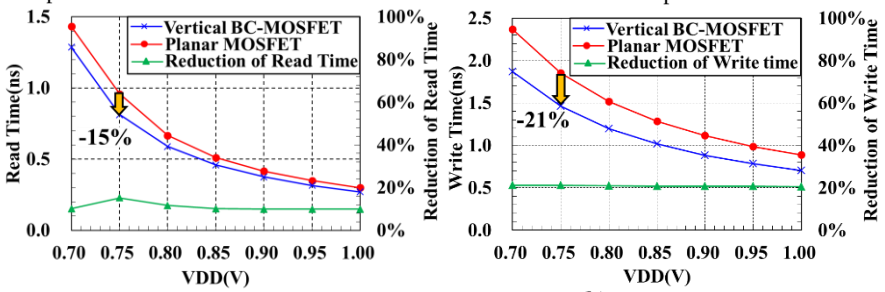


Fig. 6 Simulated leakage of a 6T SRAM cell with the Vertical BC-MOSFET and the planar MOSFET.



(a) Read time (b) Write time

Fig. 7 Simulated Read/Write time of the 6T SRAM cell array with the Vertical BC-MOSFET and the planar MOSFET.

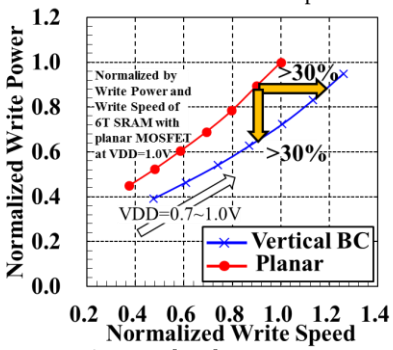


Fig. 8 Normalized write power vs. normalized write speed.

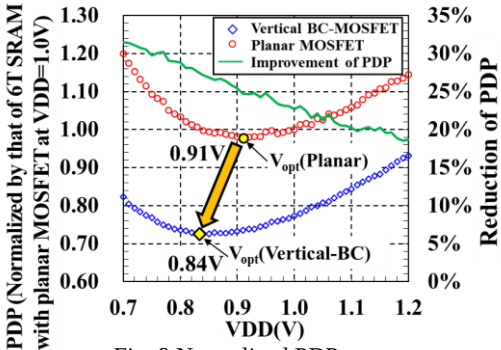


Fig. 9 Normalized PDP vs. supply voltage VDD.

Table I Benchmarking table of the 6T SRAM cell array at VDD=1.0 V.

Type of MOSFET	Planar	Vertical BC	Improvement
SNM(V)	0.383	0.407	+6.3%
RSNM(V)	0.171	0.186	+8.8%
WM(V)	0.339	0.394	+16%
Leakage(nA)	0.446	0.049	-89%
Read Time(ns)	0.300	0.270	-10%
Write Time(ns)	0.887	0.705	-21%
Write Power(μW)	0.602	0.571	-5.1%
PDP(fJ)	0.534	0.402	-25%