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The Experimental Observations of a New Dielectric-fuse Breakdown in a Bilayer-RRAM Devices to Realize the OTP Functionality

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Abstract- An RRAM realizes switchable states between SET/RESET by the modulation of filament conduction. However, RRAM maintains its window in a small range between 10X and 100X which suffers from serious disturbances of switching states during operation. To realize a much larger window, especially for the OTP functionality in a RRAM device, we proposed a dielectric-fuse(dFuse) breakdown mechanism used in RRAM structure, which results in a fairly large window (10^5-order) and is immune to the disturbance of applying voltage. To understand the formation of dfuse breakdown, random-telegraph noise (RTN) technique has been applied to illustrate the progression of the filament path with evolution of time. The results show that the path behaves like a cone, widening at the bottom electrode and narrowing on the top, with a neck and waist near 2 electrodes. More interestingly, the neck of this corne-shape filament is broken during the reset and set, but its waist is ruptured during the dFuse state.

1. Introduction

Embedded memory has a strong demand in IoT era. OTP has become the most promising one for its easy and cost-effective integration on SoC and excellent data-retention. Many solutions can realize the functionality of OTP, including the electro-migration of metal/poly liner, dielectric hard-breakdown and dielectric-fuse(dFuse) breakdown in a gate MIS of CMOS devices [1-3]. However, if one would like to implement RRAM as OTP by the conventional existing SET/RESET operations, the high disturbance between high-resistance-state (HRS) and low-resistance-state(LRS) will make an unstable storage and raise the issue of retention degradation [4]. The main concept of this work is to understand how bilayer RRAM can become an OTP by using dielectric-fuse (dFuse) breakdown mechanism. The mechanism of dFuse and other operations, including set and reset in RRAM to perform the functionality of OTP will be firstly extensively studied by using an RTN profiling technique, and the generation and evolutions of these forms during operations will be extensively studied. As a result, these new understanding of filament-formation mechanisms will be a foundation to implement the OTP by using ion-vacancy based conduction mechanisms.

2. Device Preparation

A bilayer RRAM has been prepared by stacking a 6nm HfON on 1nm Al_2O_3 between TiN as the top electrode-TE and Pt as the bottom electrode-BE before a 400^0C and 3 minutes post-metal-anneal to enhance the quality of devices, Fig.1. The area of device is $0.1\mu m^2$.

3. Results and Discussion

A. A Dielectric-fuse Mechanism in MIM structure

Fig. 2 is DC sweep of dfuse-RRAM characteristics. Except for regular SET & RESET, we apply a higher but a short pulse to RRAM, and its current is abruptly dropped from a steep cliff (the blue curve) and cannot be recovered again, similar to dielectric-fuse breakdown found in HKMG CMOS devices [3]. What happened here is that the thinner layer, Al_2O_3, creates a destructive breakdown so that Al_2O_3 dielectric becomes porous and cannot conduct the electrostatic anymore. Therefore, between TE and BE, no current flow was measured. We call this dielectric-fuse (dFuse). Moreover, we observed an abundant of RTN traps (Fig. 3), and it is believed that RTN traps are deeply involved in transition mechanisms of RRAM states. RTN technique was then applied to observe the generated traps which are closely related to the measured zig-zag waveform in Fig. 4 and a two-level waveform as shown in Fig. 5, which represents an electron trapping or detrapping by a trap in RRAM MIM. When the trap captures an electron, current increases correspondingly-τ_c; while the current reaches to a low level, an electron is then released from this trap-τ_e. RTN traps interact with electrons through trap-assisted tunneling in RRAM filament, which can be used to trace the filament path. So, after a stressing duration of a dielectric, RTN signals are gathered in step-up voltages until the resistance state is switched [3,5].

B. The Observation of Filament During Forming

Fig. 6(a) is RRAM forming-filament profile. They can be grouped into 2 trap-accumulation paths induced by electrons (the red) and vacancies (the blue) respectively. The electron-induced path interacts with TE, while the vacancy-induced path interacts with BE, which can be proved by Fig. 6(b), in which the slope of the electron-induced one is positive, and the slope of the others is negative. Between both paths, the filament is formed in the grey area of Fig. 6(a). Fig. 6(c) shows the changes of current amplitudes of RTN traps in the filament of Fig. 6(a). 2 critical regions exhibit the giant amplitudes of RTN signals, (e.g., $\Delta I_t/I_{t,high}$>40%). One of these critical regions is near TE, called "the neck", and the other is close to BE, called "the waist". Therefore, it is reasonable to assume that the current in filament will be cutoff once the neck or the waist disappears because the amplitude of the RTN traps is largely induced. Moreover, the neck length in this profile of forming filament is about 1.1nm, which is in good agreement with the previous reported results, Fig. 6(d) [6-9]. Fig. 6(e) shows the measured current transient with evolution of time, in which the process of filament generation can be divided into 4 phases, from initial sparse-and-discrete trap distribution to form small and sub-group paths, finally the complete filament formation.

C. The Observation of Filament During RESET/SET

RESET procedure has been demonstrated in Fig. 7. The neck is broken in the reset-filament profile; the neck length is ~1.5nm, which is induced by vacancy-recovery from back-diffused oxygen ions in TiN of TE. The broken neck causes HRS for RRAM. On the other hand, in the SET operation, Fig. 8, the filament growth is different from those originally created filament paths during the forming and RESET, and the SET filament path between the red and blue curves converges from the original forming-created broader filament (the grey region) to a narrow terminal at the bottom electrode. This is because, at the beginning, the values of resistance are kept at a relative low level but gradually increase and converge to a more stable high level state during cycles.

D. The Observation of Filament During dFuse

Let's revisit the blue curve in Fig. 2. By applying a higher voltage pulse on the RRAM device, a dielectric-fuse phenomenon can be observed. Accordingly, we can expect more numbers of traps in the filament during dFuse process. The results are revealed in Fig. 9 where many traps were circled around thin Al_2O_3 dielectric and the interface between HfON and Al_2O_3, and the dielectric around this region will be burned-out, yielding to the breakdown of the dielectric. This is why we measured a very low current-level in Fig. 2. In other word, "the waist" of the filament for RRAM is damaged and ruptured, such that the overall MIM structure is considered as open and can be set to the state of "0". On the other hand, the state of "logic-1" is easy by keeping the MIM at the SET condition, i.e., low resistance state (LRS). Table 1 summarizes the above three mechanisms and their comparisons of the filament structure.

In summary, a new physical mechanism, called dFuse, has been implemented in an MIM structure that has been able to provide a larger window of 10^5 times in an OTP memory. Based on a unique technique that we developed before, named Ig-RTN transient, the profiling of traps as a function of time can be achieved. Results demonstrated that the filament of RRAM can be experimentally profiled as a cone-shape path with the neck near TE and the waist close to BE. Three kinds of operations, SET/RESET/dFuse of RRAM, can be understood through the traps and the filament formation. For SET, the path near BE becomes narrower and convergent to a stable state; for RESET, the neck of the filament is broken, where the accumulated traps are filled with oxygen-ions diffusing back from TE; for dFuse, the waist of the filament has been damaged and ruptured so as not to conduct any current, i.e., an open of the path. This concept can be used to explore more application for RRAM as a potential candidate for embedded applications in the IoT era.

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References:

[1] C. E. Huang et al., ***IEEE TED***, p. 1228, 2009. [2] Y. H. Tsai et al., ***IEEE EDL***, p. 1090, 2009. [3] E. R. Hsieh et al., ***IEDM***, p. 52, 2015. [4] [5] E R. Hsieh et al., ***VLSI,*** p. 132(2015). [6] S. Yu et al., ***IEDM***, p. 413, 2011. [7] X. Lian et al., ***ICSICT***, 1-4, 2014. [8] S. Yu, et al., ***IEDM,*** p. 585, 2012. [9] G. Bersuker et al., ***IEDM***, p.456, 2010.

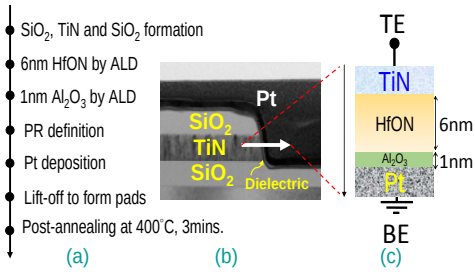


Fig. 2 Preparation of Bilayer RRAM: A bilayer RRAM structure with HfON/Al_2O_3 **(a)** The process flow, **(b)** The TEM cross-section, and **(c)** The composition of RRAM cell from TE(top-electrode) to BE(bottom-electrode).

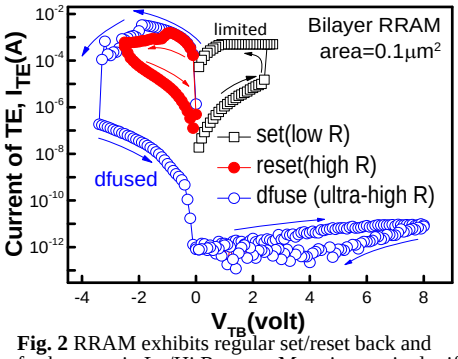


Fig. 2 RRAM exhibits regular set/reset back and forth sweep in Lo/Hi R states. More interestingly, if biased at higher electric field, the current is dropped rapidly and becomes unrecoverable.

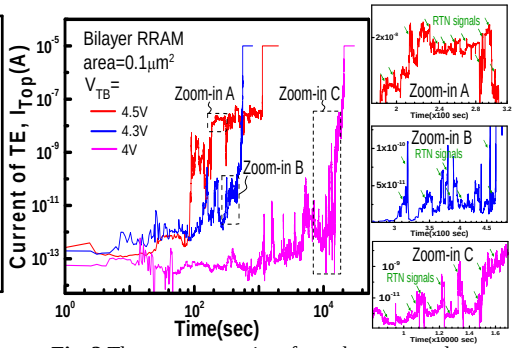


Fig. 3 The current transient from the measured current through the MIM. Lots of RTN signals are detected during current transition, which implies the strong interaction between RTN traps and current conduction.

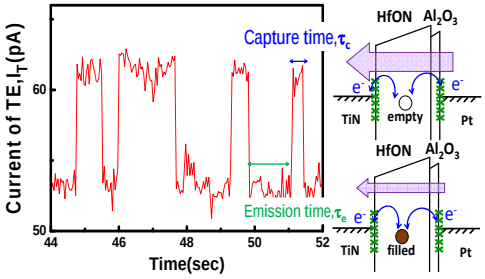


Fig. 4 To identify the mechanisms in the dielectric layer, I_T-RTN is used to locate traps during the breakdown process. I_T is low as electrons are trapped, τ_e; otherwise, it will be high when traps are empty, τ_c.

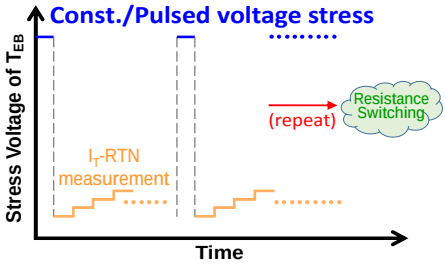


Fig. 5 Methodology of profiling RTN traps in a filament-path: A method to find the filament path by the tracing of RTN traps. First voltage stress is applied and hold. Then, RTN measurement is performed. The process is repeated until the RRAM is switched.

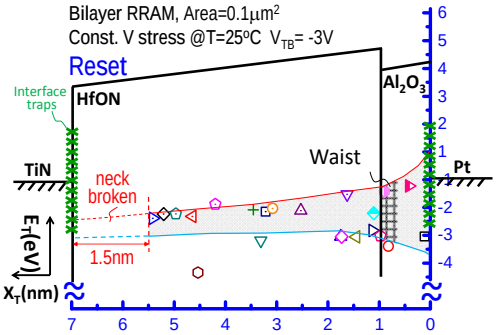


Fig. 7 The filament during Reset : The symbols are those generated traps as time progresses. After reset, the RTN traps are filled by the oxygen ions from TiN and the filament neck is broken, which decreases the conducting current and changes the resistance of RRAM to high-resistance-state (HRS).

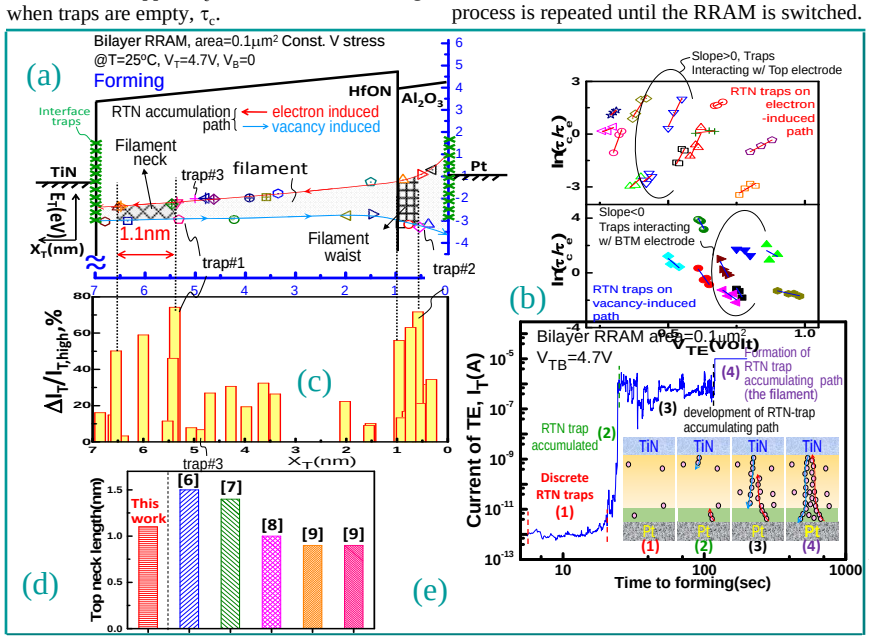


Fig. 6 (a) The forming path profiled by RTN traps. Two trap groups are found. One(the red path) conducts from Pt to TiN induced by electrons since this group almost interacts to TiN, with the positive slope of **(b)-*top***; the other(the blue path) conducts in the other direction induced by vacancies because this group exchanges electrons from Pt, with the negative slope of **(b)-*bottom***. **(c)** By observing RTN-signal amplitudes, two critical positions show giant amplitudes,(traps#1&2), which indicates that if the traps at both positions disappear, the filament will be cutoff and can not conduct current. Thus we define these positions as the neck(near TiN) and the waist(near Pt).**(d)** the neck length can be extracted from (c), which shows good matches to the references. (e) At every stage of filament growth, trap generations are shown in 4 stages(inset).

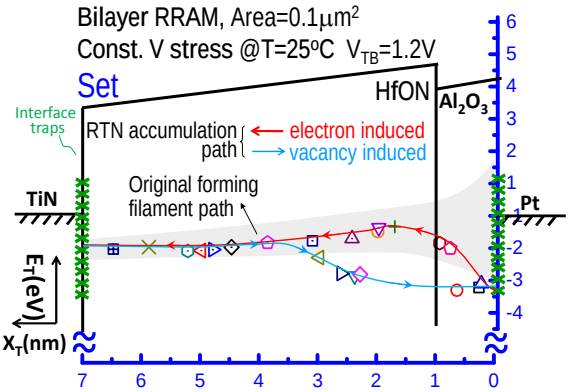


Fig. 8 Filament formation during SET: Different from the reset, the trap generation path is shown in red and blue colored lines and the filament is formed and connected the top- and bottom-electrode.

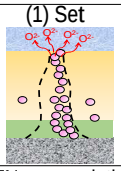
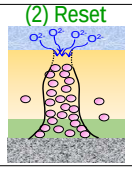
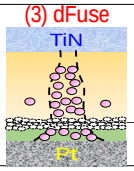
Property \ Type	(1) Set	(2) Reset	(3) dFuse
			
Switching mechanism	RTN accumulation path induced by electrons and vacancies	Repair of top broken neck by Oxygen ions	destruction of the dielectric interface (dFuse)
Operation Voltage(VTB)	2~3	-2~-3.5	> -4
path	A Filament with a neck & waist	A broken-neck filament	A broken-waist filament

Table 1 Summary of operations in Bilayer RRAM: From RTN traps, filaments can be observed for 3 different conditions, Set, Reset, and dFuse.

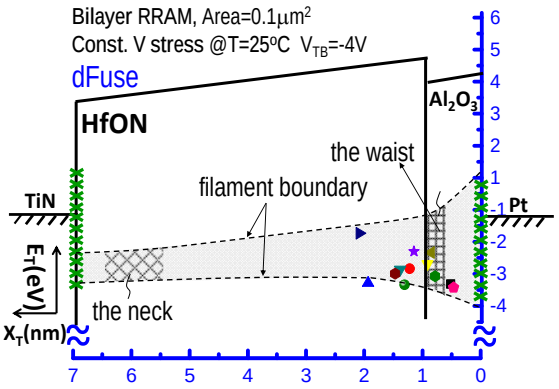


Fig. 9 Mechanism of dfuse : RTN traps during dielectric-fuse process is localized around the waist(Al_2O_3 and the interface), such that this local region was ruptured and became porous, resulting in a low conducting between the two electrodes.