

Error Free Physically Unclonable Function (PUF) with Programmed ReRAM using Reliable Resistance States by Novel ID-Generation Method

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Abstract

A stable and reliable physically unclonable function (PUF) implemented with resistive random access memory (ReRAM) is presented. This robust ReRAM-PUF uses initial resistance state and set resistance state to realize excellent stability and wide read margin, eliminating bit flipping problem at very high temperature (up to 250°C). These two stable resistance states enable stable operation at automotive environments from -40°C to 125°C without need of temperature compensation. The true randomness of PUF can be achieved by implementing a proposed ID-generation method. Most suitable forming condition can move 50% of the cells to low resistance state and the remaining 50% remain at initial high resistance state. The features of uniqueness and high reliability were experimentally verified by Hamming Distance (HD) evaluation and temperature stresses. The number of reproduction was measured to exceed 10^7 times with 0% bit error rate (BER) at read voltage from 0.4V to 0.7V.

Introduction

Physically unclonable function (PUF) is used as hardware security key to achieve authentication. Every PUF based on intrinsic properties needs to be highly unique and robust. Performance of PUF can be evaluated by Hamming Distance (HD), i.e., the inter-HD is for uniqueness and intra-HD is for reliability [1]. Several kinds of PUFs were reported to improve the security level compared with conventional non-volatile memory solutions. However, these PUFs suffered high bit error rates due to the thermal noise, voltage variation, and other aging effects [2-4].

The small cell size of ReRAM makes it a good candidate for PUF application. The undesirable variability of ReRAM could be utilized as an original source of randomness. Previously, using ReRAM's high resistance state (HRS) or low resistance state (LRS) to generate chip identity was used as the ID-generation method in PUF. HRS is chosen because of its wider resistance distribution from the random nature of ReRAM variation. The most critical problem in HRS based PUF is serious bit flipping issue under different magnitudes of reading voltage fluctuation and temperature/aging effect [1]. The LRS based PUF exhibited good performance in automotive environments, but still needs complex temperature compensation to reduce its bit error rate (BER) [5].

This paper reports a error free ReRAM-PUF with reliable resistance states by a specific ID generation method which enables high uniqueness. Furthermore, it needs not use any error correction code (ECC) to compensate for noise induced data instability or aging degradation.

ReRAM-PUF Structure and Operation

The PUF was implemented with a WO₃ based ReRAM technology (Fig. 1). The WO₃ based switching layer was formed on a W plug and PVD-TiN was deposited as top electrode (Fig. 2). To generate reliable PUF-ID with highest randomness and bias/temperature/aging reliability, a novel FORM+SET operation was proposed based on the ReRAM switching mechanism. The cells successfully formed can be set to low-resistance state due to the creation of conductive filaments (CF) of oxygen vacancies. On the other hand, the cells not being formed can not be set to LRS and therefore stay at initial high-resistance state (Fig. 3). The operation flow to generate the PUF-ID suitable for mass production is shown in (Fig. 4). Successfully-formed bits and not-formed bits are scattered in an array after applying a meta-forming pulse condition due to the random nature of ReRAM. After the forming operation, a set pulse was applied to all cells and the robust ReRAM-PUF ID was generated with initial HRS cells and LRS cells. These two reliable resistance states exhibited excellent immunity against automotive environment. Most suitable forming condition can move 50% of cells to LRS, which provides the best randomness and eliminate the chance of duplication. The forming rate can be controlled by the forming voltage to get highest degree of randomness (which is at 50%). We demonstrated that under different process

conditions and different technology nodes the forming rate could be well-controlled by the applied voltages (Fig. 5a). Applying multiple constant forming pulses when approaching the target could further fine tune the forming rate effectively (Fig. 5b). It is promising that ReRAM-PUF with small contact size and suitable thickness of switching layer can be applied to advanced CMOS technologies.

Resistive ranges of 64 bits memory cells showed plentiful read margin between set state and initial state after the ID generation. We chose a fixed threshold (TH) of 700K-ohm to distinguish data 0 and data 1 (Fig. 6). The resulted bit map after SET operation represented a PUF ID in binary code and could be translated to hexadecimal code (Fig. 7). For uniformity evaluation, the occurrence counts and probability for the first 3 bits response from 16K different 64-bit codes on a 1Mb test chip were analyzed (Fig. 8). The uniform occurrence probability originated from the intrinsic randomness of ReRAM was shown. A ReRAM cell of the PUF after SET operation was examined by a high-resolution TEM (Fig. 9). It showed that the filament was hard to detect by an invader. Therefore the ReRAM-PUF can provide high security.

Performance of the ReRAM-PUF

The PUF-array can be enlarged from 64 bits to 1K bits for strong PUF application. The plentiful read margin with best randomness of data 0/1 was also demonstrated in 1Kb responses (PUF codes) (Fig. 10). The uniformity distribution of 1kb responses with data 1 implemented on a 1Mb array was measured. The distribution was centered at 48.84% with low standard deviation (σ) of 2.96% when optimized forming condition was applied (Fig. 11a). The inter-chip HD for uniqueness was also evaluated. The distribution was centered at 50.04%, very close to ideal value of 50%, and the standard deviation was 1.62% (Fig. 11b). Resistance range of 1K-bit memory cells under different temperature from -40°C to 125°C showed excellent stability and the inset exhibited 0% failure rate with read voltage from 0.4V to 0.7V (Fig. 12). The robust retention after baking at 250°C for 65hrs was also demonstrated (Fig. 13). The bit mappings showed 0% BER before and after the baking (Fig. 14). Based on measured averaged resistances of worst case tail bits from 0.001% to 0.05% in 1000 1Kb codes at 210°C over about 65 hours, we predicted that a retention of 10 years at 210°C was possible (Fig. 15). The number of reproduction (read) at different read voltages were confirmed to be more than 10^7 times with 0% failure (Fig. 16). Inter-PUF and Intra-PUF evaluations with unlimited separation of HD were carried out to show good uniqueness and robustness of the ReRAM-PUF (Fig. 17). The intra-PUF HD is the relative HD between the responses measured on the same PUF chip at various times under varying conditions. The worst case of intra-PUF was considered in this case. The ideal 0% BER for intra-PUF was achieved successfully even the ReRAM-PUF was under the corner operation conditions. The measured results of our ReRAM-PUF showed good performance and high security compared with other published PUF devices (Table. I).

Conclusion

Using a unique ID-generation method, our ReRAM-PUF can provide two reliable resistance states with high read margin for robust PUF application. The excellent PUF performance including high uniqueness and robust reliability without error correction code was presented in this paper. The ReRAM-PUF is suitable for secure ID generation in consumer, enterprise, automotive, and military products.

References

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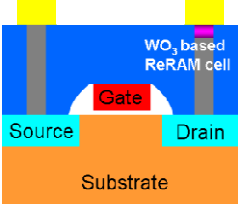


Fig.1. Schematic of a 1T1R structure with WO_x switching layer.

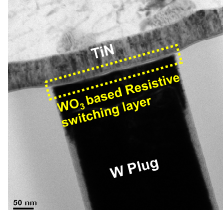


Fig.2. Cross-sectional TEM image of the WO_x based ReRAM.

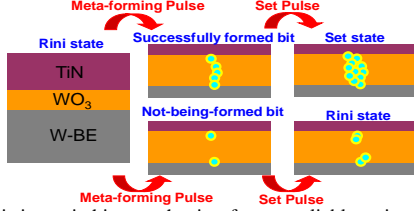


Fig.3. Resistive switching mechanism for two-reliable-resistance formation.

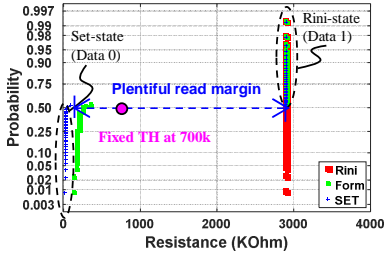


Fig.6. Resistive ranges of 64 bits memory cells resulted from using the proposed ID-generation method.

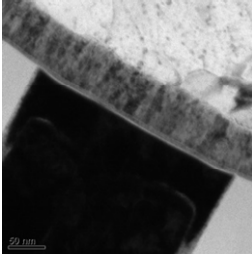


Fig.9. Cross-sectional TEM image of the ReRAM-PUF after set operation.

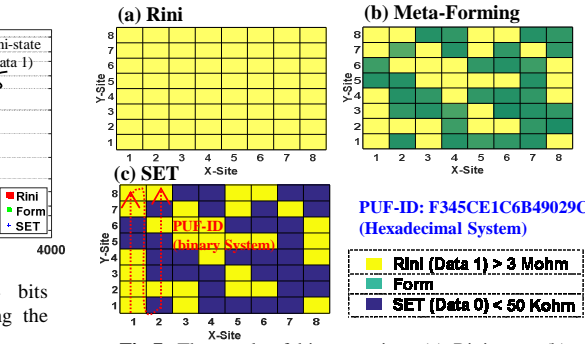


Fig.7. The result of bits mapping: (a) Rini state (b) After a meta-forming pulse (c) After a set pulse.

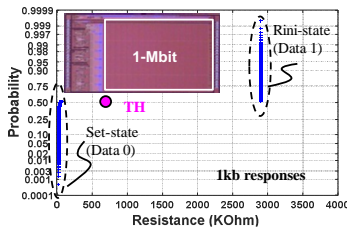


Fig.10. Resistive range of 1-Kbit array. The inset shows 1-Mbit ReRAM array.

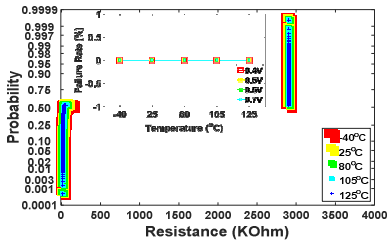


Fig.12. Resistive range of 1k bits memory cells before and under -40°C to 125°C. The inset shows 0.00% failure rate under different read voltages.

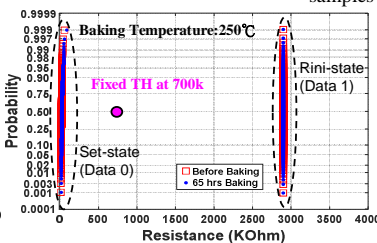


Fig.13. The robust retention before and after high temperature 250 °C baking test.

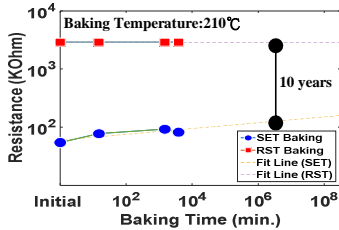


Fig.15. 210 °C retention test of tail bits from 0.001% to 0.05% in a 1K-bit distribution.

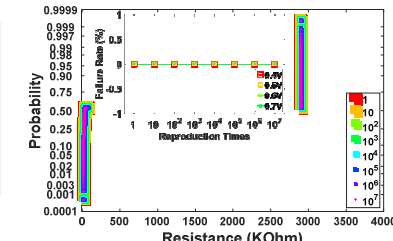


Fig.16. Resistive range of 1k cells after different numbers of reproduction. The inset shows 0% failure rate under different read voltages.

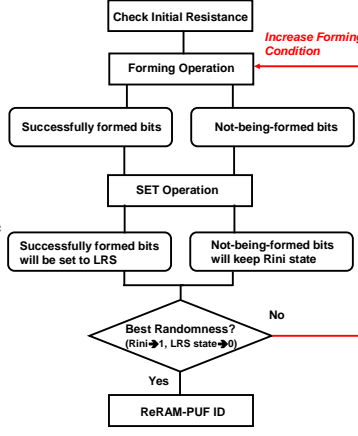


Fig.4. Proposed ID-generation algorithm.

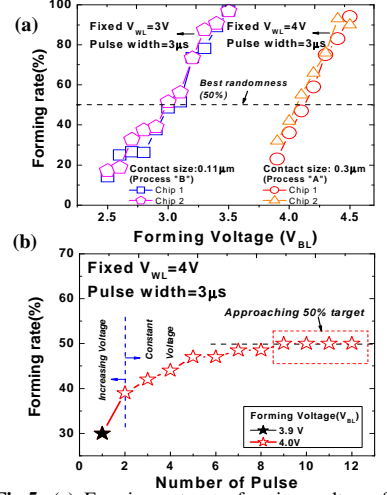


Fig.5. (a) Forming rate vs. forming voltage for different contact sizes and processes. (b) Forming rate vs. number of pulse by constant voltage.

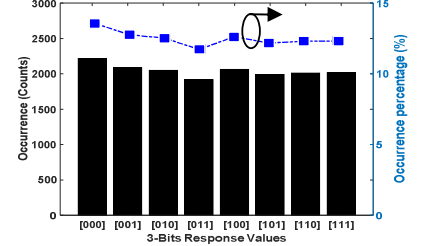


Fig.8. The occurrence counts and probability for the first 3 bits response of 64 bits on a 1Mb array.

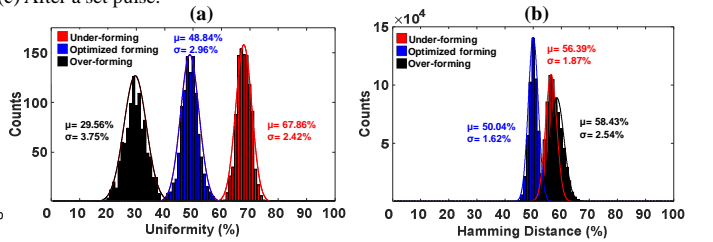


Fig.11. (a) The uniformity of 1kb responses with data 1 and different forming condition implemented on 1Mb array (b) The inter-HD distribution with 1k samples and different forming condition measured by 1kb responses.

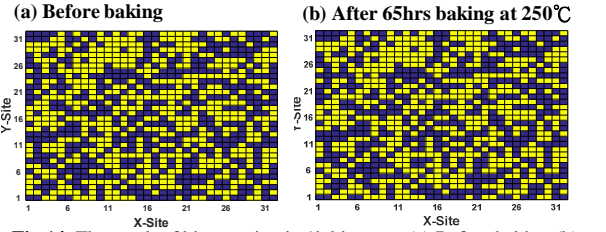


Fig.14. The result of bit mapping in 1k bit array: (a) Before baking (b) After 65hrs baking at 250 °C.

Table I. PUF comparisons

PUF Device	BER in worst case (%)	Temperature range(°C)
SRAM[1]	0.97%	25°C-50°C
PATA [2]	2%	0°C-80°C
INV-PUF[3]	1.73%	25°C-85°C
HRS based ReRAM[4]	>1%	25°C
LRS based ReRAM[5]	0.49%	-40°C-125°C
This work	0%	-40°C-250°C

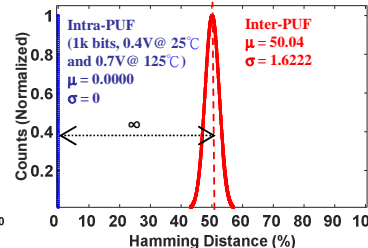


Fig.17. Inter-PUF and Intra-PUF evaluations with unlimited separation of HD.