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Highly Reliable Logic-Compatible MTP Memory for Automotive Applications

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Abstract

In this paper, a fully logic-compatible non-volatile memory structure is presented. The memory cell with unique configuration minimizes program-erase window closure and performs the endurance up to 100K cycles and excellent retention capability for automotive applications. An 8-kbits macro is also successfully demonstrated for product applications.

1. Introduction

Embedded logic MTP is known as embedded Flash memory alternative for product developers acquiring NVM function onto different process platforms, and minimizes the possible cost increase incurred by complicated process steps in embedded Flash process. However, in order to keep logic MTP fully compatible with existing processes or even to allow logic MTP migration among processes, due to intrinsic physics limitation, most of MTP technologies suffer critical challenges in Program/Erase (P/E) window closure while P/E cycle increased. With increased P/E cycles, electron traps are generated gradually at the gate-oxide/silicon interface then effectively shift flat-band voltage and reduce electric-field across gate-oxide layer during P/E operations, and also aggravate surface scattering along the read channel resulting in the trans-conductance (Gm) degradation in read operations [1]-[3]. It has also been reported the Gm and sub-threshold slope (S.S) degradations are getting worse as oxide thickness grown thicker [4], especially when ambient temperature raised. For the processes with 5V devices, like logic, HV or BCD processes with gate oxide thickness widely ranging from 11nm to 15nm, such issue significantly restricts the endurance capability in traditional logic MTP. A high endurance MTP cell is therefore introduced to alleviate the degradations so as to extend its endurance window.

2. Cell structure and its operation

The schematic and operating concepts of the proposed cell are shown in Fig. 1 and Table. 1. The cell consists of 2 capacitors (C1, C2) and 2 transistors (M1, M2) sharing one floating-gate, C1 dominates the coupling ratio to the floating gate. In Program operation, the bias of node PS enables Fowler-Nordheim (F-N) tunneling through the gate oxide in M2. In Erase operation, the bias of node EL enables F-N tunneling through the gate oxide in C2 instead. In Read operation, cell current is detected from M1. A conventional cell [1] is provided for further comparisons, as described in Fig. 2 and Table. 2. Obviously, M1 of the conventional cell has to be activated in both Program and Read operations, while M1 and M2 in the proposed one work alternately. Even with additional M2 transistor, the cell size gains only 10% larger than the conventional one's with similar layout techniques.

3. Characterization Results and Discussion

Fig. 3 show the characteristics of conventional cell after 100K cycles, which shows tremendously erase-state current decrease from 170uA to 5uA. It results from three factors: (1) the Erase efficiency degradation due to electrons trapped in C2 gate oxide, (2) Vth raise and (3) Gm degradation of M1 coming from electrons trapped in M1 gate oxide after repetitive Program operations [3]. On the contrary, Fig. 4 demonstrate the drop of proposed cell after cycling is 38uA only. Since M1 transistor of proposed cell is only activated in Read operation, no electron traps are produced in its gate oxide, hence no Gm deformation and Vth raise like the case in conventional cell in Fig. 3. Different from the conventional cell, the $Gm|_{max}$ value of program state in Fig. 4 again show no surface scattering issues after cycling. Vt of program- and erase- state shift are still found, simply because of tunneling efficiency decay, but the proposed cell mitigates erase-state current decrease commonly seen in conventional cell, as pictured in Fig 5 (a) to (d). Fig. 6 show the cycling trend up to 1 million times for current window comparison. Fig. 7 depicts $Gm|_{max}$ of program states and $Gm|_{0V}$ of erase state; the $Gm|_{max}$ tells the effects on surface scattering regardless Vt shift of read transistor, while $Gm|_{0V}$ further tells the combined effect of device degradation under a certain Read condition, 0V. Proposed cell with a monotonic increase of $Gm|_{0V}$ reflects purely Vt shift of erase-state, while conventional cell tells the impacts of those three factors mentioned above. Fig. 8(a) and 8(b) demonstrate the endurance characteristics of an 8K-bits macro cycled and read at 150°C, and Fig. 9(a) and 9(b) show a retention result of 150°C 168hr and 336hr baking, it expects to have sufficient P/E window after 150°C 10year.

4. Conclusion

A highly reliable logic-compatible MTP memory is presented for the needs of high endurance spec and high temperature operation. With such a current sensing window expanding technique, the MTP cell demonstrates fully generic process compatibility and the product competitiveness for automotive applications.

References

[1] K. Ohsaki, et al., IEEE Journal of Solid-State Circuits, vol.29, no. 3, pp. 311-316, March, 1994.
[2] P. Cappelletti et. al., in IEDM Tech. Dig., 1994, pp. 291–294.
[3] J-D. Lee et. al., in Proc. IRPS, 2003, pp. 497–501.
[4] Y.-B. Park et. al., *IEEE Trans. Electron Devices, Vol. 45, p. 1361, 1998*

Table. 1 Proposed cell's operation

MODE	CL	SL	BL	EL	PW	PS
PGM	Vp	f	f	Vp	0	0/f
ERS	0	0	0	Ve	0	0
READ	0	0	1.2	0	0	0

Table. 2 Conventional cell's operation

MODE	CL	SL	BL	EL	PW	
PGM	Vp	0/f	0/f	Vp	0	
ERS	0	0	0	Ve	0	
READ	0	0	1.2	0	0	

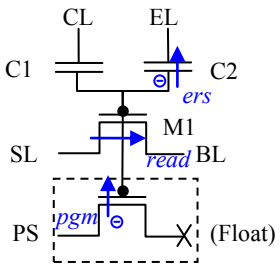

Fig. 1 Proposed cell

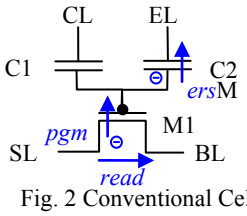

Fig. 2 Conventional Cell

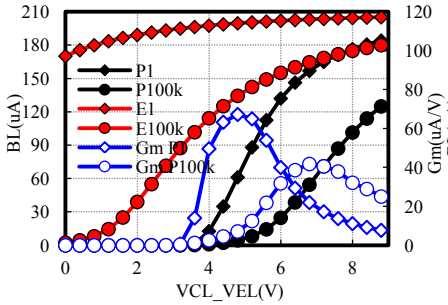

Fig. 3 Conventional cell's IV curves

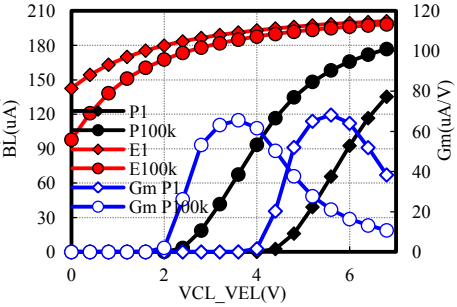

Fig. 4 Proposed cell's IV curves

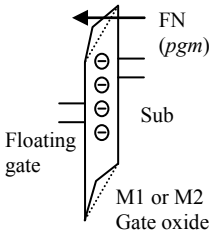

Fig. 5(a) Program band diagram

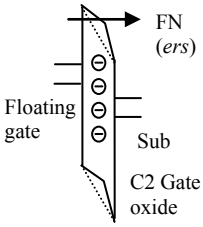

Fig. 5(b) Erase band diagram

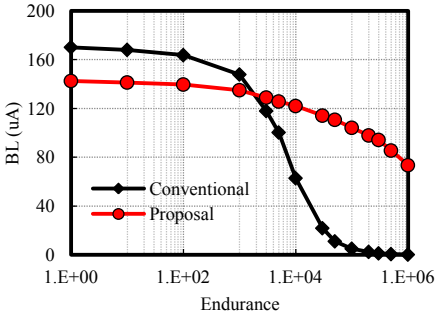

Fig. 6 BL(uA) by endurance

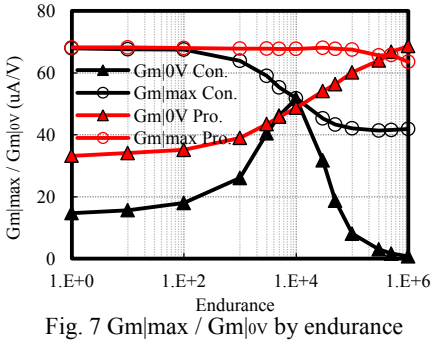

Fig. 7 Gm|max / Gm|ov by endurance

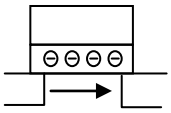
Fig. 5(c) electron traps in M1 oxide of conventional cell

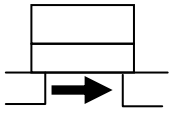
Fig.5(d) "No" electron traps in M1 oxide of proposed cell

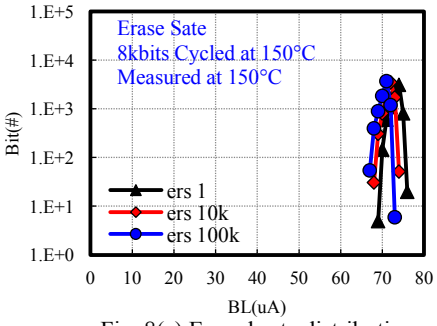

Fig. 8(a) Erased sate distribution

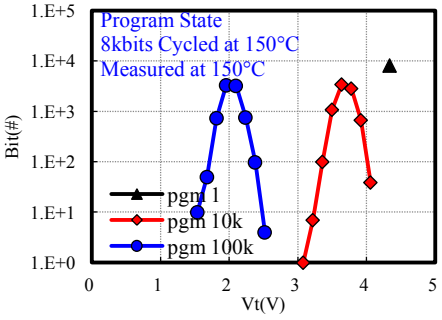

Fig. 8(b) Program sate distribution

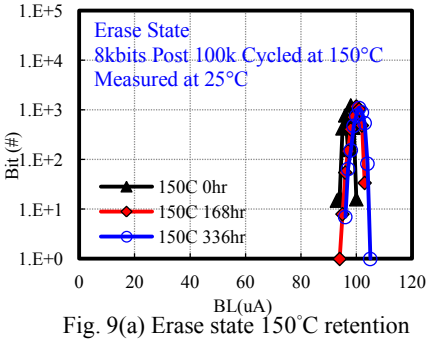

Fig. 9(a) Erase state 150˚C retention

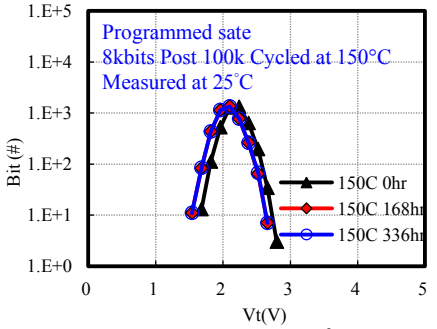

Fig. 9(b) Program state 150˚C retention