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Thermal Stability and Switching Performance of iPCM at Elevated Temperature

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Abstract

The peculiar behavior of interfacial phase-change memory (iPCM) devices switching at elevated temperature is explored. The thermal stability of the devices resistance was measured and a new resistance level of iPCM that can be used for advanced programming was found.

1. Introduction

Phase-change memory performance, appealing in many aspects, reached a new technological level with the appearance of iPCM promising a significant decrease of energy requirements and even a switching speed enhancement. These advantages stem from the specific structural architecture of the GeTe/Sb_2Te_3 superlattice that is used as a switchable structure in iPCM. Complicated effects can be expected [1,2] due to the appearance of additional GeTe/Sb_2Te_3 interfaces (leading to the formation of van der Waals gaps and the emergence of topological insulator properties) as well as the possible existence of different phases attributable to variations of the GeTe/Sb_2Te_3 layers stacking order. From this perspective it is important to address issues related to thermal stability, data retention, and the overall switching behavior of iPCM devices at elevated temperature which is a critical criteria for industrial application of memory devices. Peculiar behavior of such characteristics of iPCM devices can be expected, since even for the Ge-Sb-Te alloy phase-change memory one can obtain a significant thermal stability improvement by mere doping or with a slight composition variation [3]. In this work the switching behavior, thermal stability, and thermally induced resistance features of GeTe/Sb_2Te_3 superlattice based iPCM devices are reported.

2. Results and discussion

iPCM devices were fabricated with $[(GeTe)_2(Sb_2Te_3)_4]_8$ superlattice structures (43 nm thick including a seed layer) following the procedures described in [4]. The size of the active device area was varied from 50x50 nm to 100x100 nm. Tungsten was used for top and bottom contacts layers. The electrical switching performance of iPCM devices was tested with the use of 100-500 ns short pulses. The room temperature switching performance was found to be comparable to the iPCM performance that was reported earlier [5]. An endurance check showed switching up to 10^8 cycles. For the room temperature switching, the SET and RESET states resistance levels remained at around 10^2 and 10^6 Ohms, respectively (figure 1), this condition is labeled as a state (I).

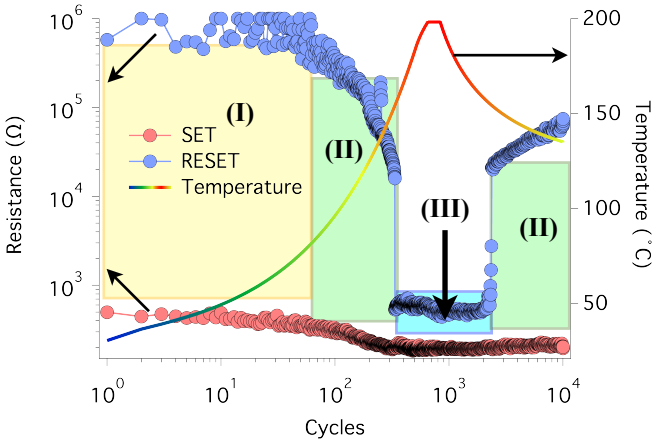

Fig. 1 iPCM device SET and RESET resistances as a function of temperature up to 200°C along with the switching behavior at every measuring point.

Subsequently, the sample temperature was increased from room temperature to 200°C using a heating stage while carrying out simultaneous switching cycling and resistance measurements. It should be noted that the two curves shown in the figure were obtained by sequential switching between the SET and RESET states using short pulses and the delay times between writing and reading pulses were long enough to let the device state be established after each writing pulse. The thermal stability of the devices was found to be reasonable, and similar to the alloy case: at around 90°C, the RESET resistance level shifted to lower values (state (II)) and finally suddenly drops more than three orders of magnitude in total (state (III)) at about 150°C. After reaching 200°C, the sample was cooled down, and the RESET resistance level was found to return to the initial room temperature value. The SET state resistance slightly decreases as well from ~90°C, while the RESET resistance doesn't attain this new SET resistance level. If the structures had been fabricated from Ge-Sb-Te alloy then the appeared feature could be explained from a thermal processes viewpoint. Namely, after the transition at 150°C, a further temperature rise could lead to the growth of crystalline grains. This would in turn lead to a decrease in charge carrier scattering at grain boundaries and consequentially an increase in carrier mobility, resulting in a decrease of the SET resistance [6]. How-

ever, the switching mechanism of the GeTe/Sb_2Te_3 superlattice is believed to be different from such a thermal model [5]. Furthermore, this speculative thermodynamic explanation of the observed resistance behavior is not valid, in light of the observed resistance behavior at the cooling process (without electrically driven switching). In fact, for the alloy case, as soon as annealing leads to a decrease in defects concentration, the device resistance should not change during cooling [7]. However, the resistances of the SET and RESET states in iPCM devices annealed without electrically driven switching behave differently: the RESET state resistance remains nominally the same ($\Delta R \approx 20\Omega$) with a temperature decrease from 180˚C to ~110˚C (figure 2, top panel),

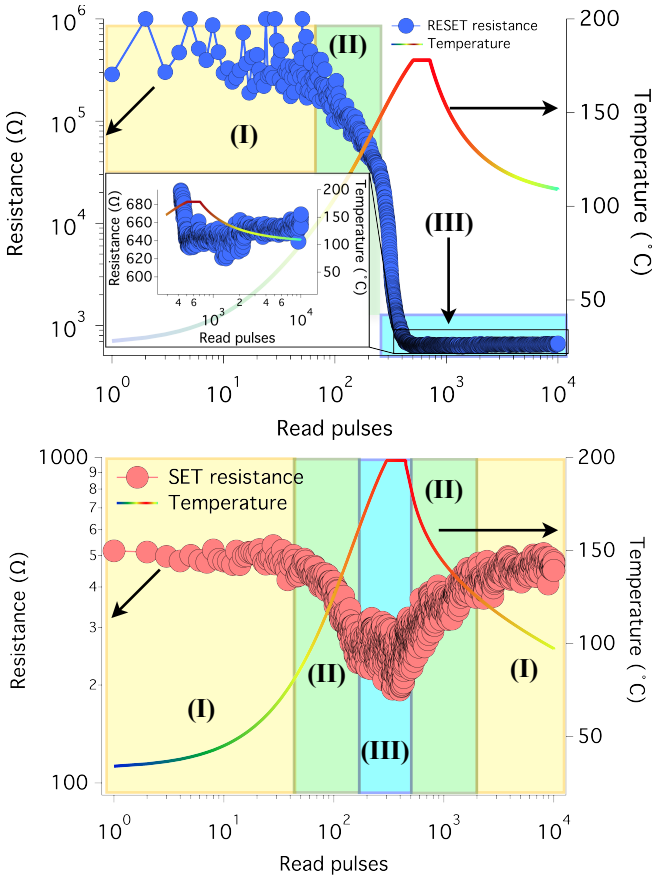

Fig. 2 iPCM device RESET (top panel) and SET (bottom panel) resistances as a function of temperature up to 180 ˚C and 200˚C correspondingly without electrically driven switching.

while the SET state resistance recovers to its initial state by ~120˚C with $\Delta R \approx 300\Omega$ (figure 2, bottom panel). Therefore, the observed resistance behavior indicates that the SET/RESET states of the superlattice-based iPCM devices are not the same as in Ge-Sb-Te alloy, and the nature of the electrically induced switching in the former devices is at least not purely thermal. This peculiar behavior of the superlattice switching at elevated temperature can be explained by the existence of several different phases in the GeTe/Sb_2Te_3 structure. This effect ultimately can be used in multilevel memory devices, especially since it was found that the initial levels of the SET and RESET resistances recover after the cooling process and a consequent write-erase cycle. The obtained data can be used to build a map of the iPCM switching thermal stability (figure 3): the preferable temperature region for iPCM operation is below 100 ˚C, allowing

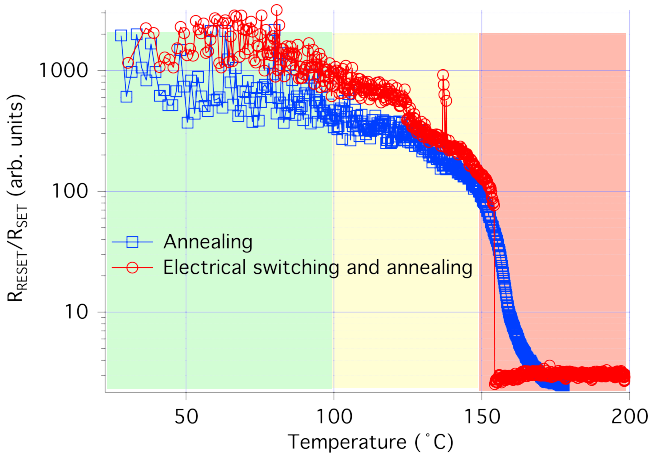

Fig. 3 iPCM device RESET to SET resistances ratio data as a function of temperature. Colored areas of the plot reflect different memory operation temperature regions.

for nearly three orders of magnitude in the resistance differential between the SET and RESET states. From 100˚C to 150˚C as soon as thermal effects begin to play a significant role, the resistance ratio decreases by two orders of magnitude, which is, in principle, sufficient for some applications. Finally, devices cannot be switched for temperatures higher than ~150˚C in a conventional manner, which is therefore serves as a limit for the operation of iPCM devices discussed here.

3. Conclusions

The behavior of the GeTe/Sb_2Te_3 superlattice-based iPCM devices switching and the thermal stability at the elevated temperature up to 200˚C was studied. The appearance of additional resistance levels in iPCM at T>150˚C was found.

Acknowledgements

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