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Programming Current Reduction in GeS_2+Sb_2Te_3 Based Phase-Change Memory

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***Abstract*—In this paper, we study the functionality of Phase-Change Memory (PCM) based on GeS_2+Sb_2Te_3 alloys (GSST). GSST PCM cells show data retention of one hour up to 290°C. RESET current is reduced by one decade wrt to standard $Ge_2Sb_2Te_5$ thanks to the enhanced thermal resistance of the devices and the likely decreased active volume involved in the phase-change transition. These results enable GSST based PCM as a suitable candidate for low power applications.**

***Index Terms*— PCM, Phase-Change Memory, GeS_2/Sb_2Te_3, low power applications.**

I. Introduction

Phase-Change Memories (PCM) are among the most advanced Resistive Non-Volatile Memory (NVM) technologies. PCM with fast access time, high read and write throughput, good data retention, bit alterability and good endurance performance have been recently demonstrated [1]. Nonetheless, programming current reduction is required in order to address ultra-low power applications.

Thanks to the phase-change material engineering, a great reduction of the programming current was achieved introducing a non-crystalizing material inside the active volume of the device, in a so-called Intergranular Structure (IG) [2]. In the light of these recent results, we propose in this paper the investigation of an innovative compound material based on GeS_2 + Sb_2Te_3 (GSST). GeS_2 has been used as an amorphous surrounding material for Cu in CBRAM applications [3], showing a high resistivity and being porous. Whereas Sb_2Te_3 is known to be highly conductive, featuring a high crystallization speed as well as a low stability of its amorphous phase [4]. In this paper, three GSST compounds are explored with an increasing amount of Sb_2Te_3 (henceforth, referred to as material GSST-A, -B and -C). Thanks to the physico-chemical analyses we highlight the particular crystallization dynamics of GSST. Conduction mechanisms as well as electrical performances are investigated in GSST based PCM cells, showing how the reduced active volume and the increased thermal resistance of the devices lead to a reduced programming current and improved thermal stability at high temperature wrt standard $Ge_2Sb_2Te_5$ (GST).

II. Physico-chemical Analysis of GSST Materials

Resistivity-vs-Temperature characterizations of full-sheet GSST materials (**Fig. 1**) reveal a strong improvement of the thermal stability of these layers wrt Sb_2Te_3. GSST-A and -B present a high resistivity up to 450°C (comparable to GeS_2). On the contrary, compound C (the one with the highest content in Sb_2Te_3) shows the same resistivity as materials A and B at room temperature before to trigger the crystallization at approximately 260°C. The XRD analysis (**Fig. 2**) confirms the absence of crystal patterns in the 'as deposited' GSST-C sample, while the typical peaks of crystalline Sb_2Te_3 appear after thermal annealing at 400°C. TEM analyses performed on GSST-C reveal a uniform layer after deposition, while crystalline filaments appear after annealing at 400°C, surrounded by fully amorphous regions (**Fig. 3**). As reported in [5], we believe that the reduced size of Sb_2Te_3 regions in GSST samples correlates with their improved stability at high temperature observed in the resistivity analysis.

III. Electrical Characterization of GSST PCM

GSST layers were integrated by magnetron sputtering in a relaxed PCM lance-type structure with a 300 nm wide tungsten based bottom electrode. Electrical results were compared to the ones obtained on GST cells based on the same structure. The quasi-static IV curve (**Fig. 4**) of GST in the SET state shows an Ohmic behavior while RESET state shows a Poole-Frenkel like (PF) conduction at low electric fields (E) and a regime of high field dependency at high electric fields. On the contrary for both SET and RESET state in GSST-C we observe the same dependency on E even at high electric fields that we think it can be correlated with a percolation model of conduction [6].

GSST needs higher voltage for the first initialization wrt the threshold voltage (V_{th}) used during later programming (**Fig. 5**). Furthermore, we observe a reduction of V_{th} and of its std. deviation for an increasing amount of Sb_2Te_3, likely correlated to the lower stress induced in the devices thanks to the lower voltage required during the initialization.

Compared to std. GST devices, the RESET current (**Fig. 6**) of all the three GSST is reduced by one order of magnitude. Additionally, the SET and RESET resistances shift to higher values. This result supports the hypothesis of a confined active material in an amorphous matrix as schematized in **Fig. 7**.

Endurance performances are greatly improved for an increasing amount of Sb_2Te_3 (**Fig. 8**). Being endurance correlated with the total programming energy, lower voltage operations demonstrated in GSST-C could explain the achieved result.

In **Fig. 9**, the SET speed of GSST-C is displayed by a Shmoo plot. The speed is slowed down compared to pure Sb_2Te_3 [4], but comparable to other materials of state-of-the-art PCM devices [7]. GSST-C and GST samples were programmed in both SET and RESET states and annealed at increasing temperatures. While GST RESET cells crystallize at 180°C, GSST cells keep a resistance window of one order of magnitude up to 290°C **(Fig. 10)**. Finally, we evaluated the thermal resistance (R_{th}) of GSST-C and GST devices from the calculated melting power at different working temperatures (**Fig. 11**) [8]. GSST-C shows a higher R_{th} wrt GST that coupled with the smaller amount of active volume in the device contributes to the found reduction of the programming current. Moreover, a higher thermal resistance is suitable for high density memory arrays to avoid thermal crosstalk during programming.

IV. Conclusion

We have analyzed the functionality of innovative GeS_2 + Sb_2Te_3 (GSST) based PCM devices. A data retention of one hour up to 290°C was demonstrated. We showed a reduction of the RESET current by one decade wrt to standard GST thanks to the enhanced thermal resistance achieved in GSST devices and the likely decreased active volume involved in the phase change transition. These results enable GSST based PCM as a suitable candidate for high density memory arrays targeting low power applications.

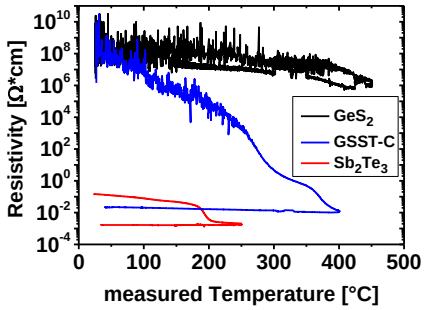

Fig. 1: Resistivity-vs-Temperature characteristics of GSST materials compared to GeS_2 and Sb_2Te_3 (GSST-A and -B are not reported due to overlapping with GeS_2)

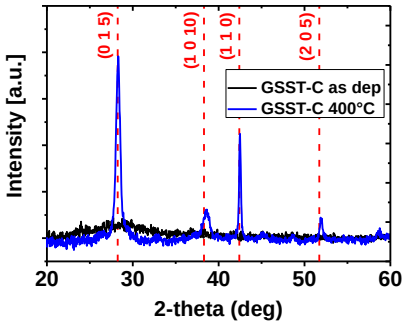

Fig. 2: XRD measurement of GSST-C as deposited and after annealing at 400°C.

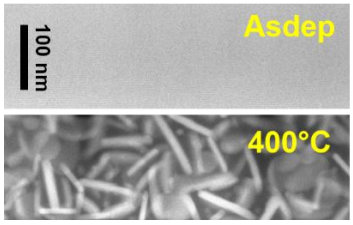

Fig. 3: TEM analysis of GSST-C as deposited and after annealing at 400°C.

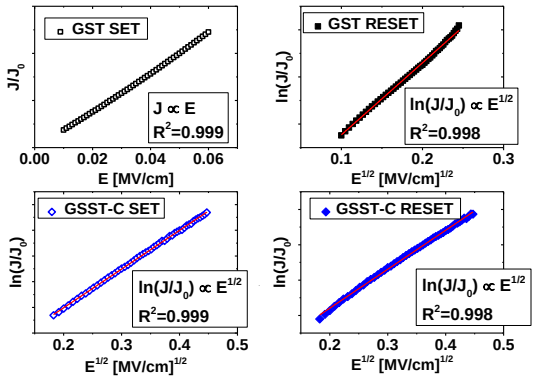

Fig. 4: Quasistatic IV curves below V_{th} for GSST-C and GST. GSST-C shows a likely percolation conduction even at high electric fields.

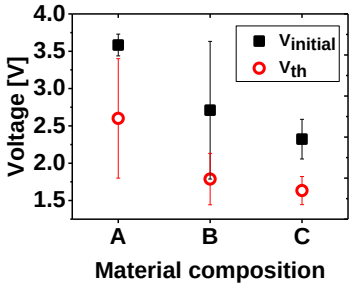

Fig. 5: Initialization voltage and V_{th} for GSST devices.

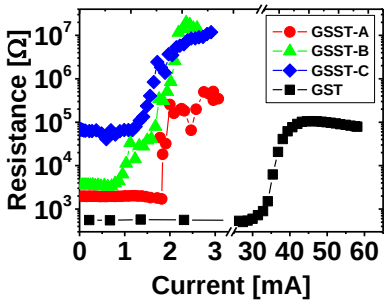

Fig. 6: Resistance-vs-Current for the three GSST wrt GST. RESET current is reduced by one decade in GSST devices.

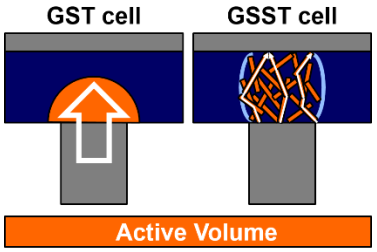

Fig. 7: Scheme describing the different active volume involved in the phase-change transition in GST and GSST cells.

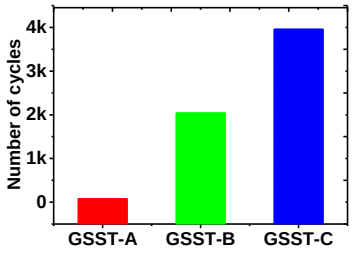

Fig. 8: Endurance results obtained from GSST devices. Higher content in Sb_2Te_3 improves the device cyclability, thanks to the reduced voltage operations (Fig. 5).

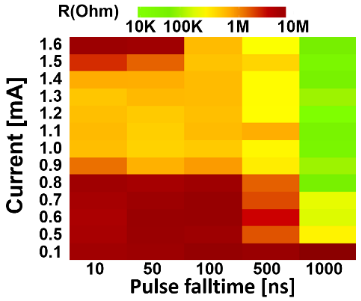

Fig. 9: Shmoo plot of SET resistance achieved with increasing fall time vs current for GSST-C (pulse width = 300 ns). SET time is in the order of 1µs.

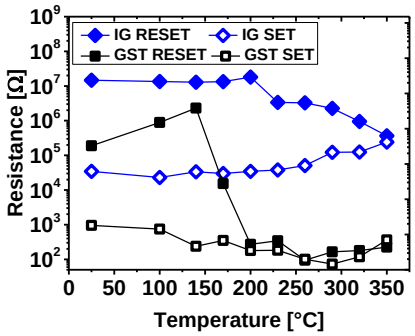

Fig. 10: Temperature stability of SET and RESET state (after annealing of 1h at each given temperature) for GSST-C compared to GST.

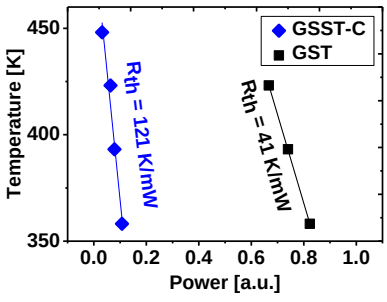

Fig. 11: Thermal resistance calcualtion for GSST-C and GST devices. GSST-C exhibits a higher R_{th}.

V. Acknowledgment

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