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Temperature Dependence of Transport Properties in dinaphtho[2,3-b:2',3'-d] thiophene Thin-Film Transistors with MoO_3/Au Electrodes

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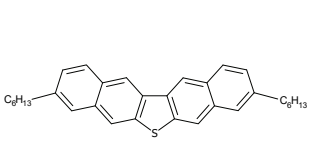
Abstract

We have investigated gate-bias and temperature dependence in C6-DNT-V TFTs by inserting MoO_3 between C6-DNT-V layer and Au electrodes. Temperature dependence voltage-current (V_D-I_D) characteristics from 133 K to 293 K with different gate-bias voltage were measured to evaluate possible charge transport mechanism in C6-DNT-V thin film. We found two possible charge transport mechanisms related to carrier injection from metal electrode and grain boundary conduction.

1. Introduction

Organic thin-film transistors (OTFTs) have recently attracted a great deal of interest for organic electronic applications, such as, flat panel displays, electronic paper, and radio frequency identification tags. In particular, hexyl-substituted dinaphtho[2,3-b:2',3'-d]thiophene (C6-DNT-V) is considered to be one of the most promising organic semiconductors in OTFTs because of its high hole mobility. Recently, study on charge transport in OTFTs has become an important subject for improving device performance of transistor. The OTFTs can be improved by inserting metal oxide, such as, molybdenum oxide (MoO_3), germanium oxide (GeO) and tungsten oxide (WO_3) between electrode/semiconductor interface. [1] In the previous work, temperature dependence in pentacene and C8-BTBT OTFTs with MoO_3/Au electrodes have been reported. [2, 3] In this study, we have investigated gate-bias and temperature dependence in C6-DNT-V TFTs by inserting MoO_3 between C6-DNT-V layer and Au electrodes. Temperature dependence voltage-current (V_D-I_D) characteristics from 133 K to 293 K with different gate-bias voltage were measured to evaluate possible charge transport mechanism in C6-DNT-V thin film.

2. Experiment



C6-DNT-V

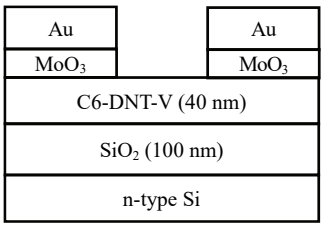
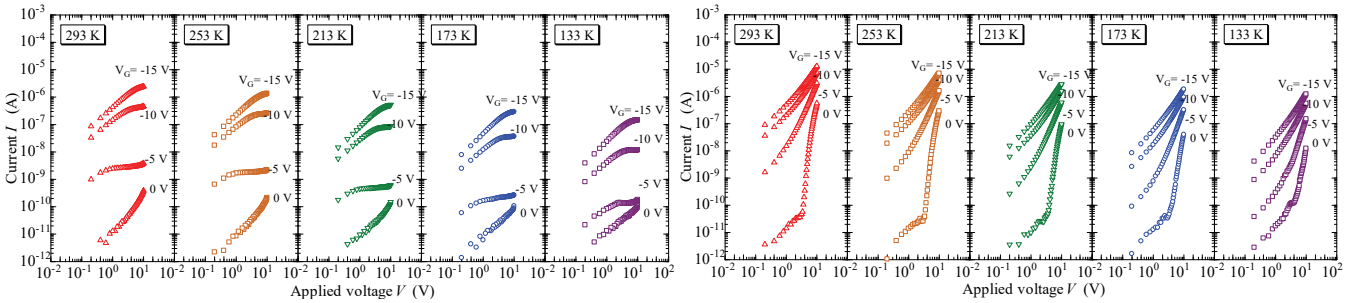


Fig. 1 Molecular and device structures of OTFTs.

The structure of the top-contact bottom-gate C6-DNT-V OTFTs fabricated in this study has been shown schematically in Fig. 1. A heavily doped n-type silicon substrate oxidized with a 100 nm SiO_2 layer was used as the substrate. The silicon substrates were cleaned in an ultrasonic bath with acetone, isopropanol, and deionized (DI) water for 5 min. The substrates were then dried with an air gun. A 40 nm thick layer of C6-DNT-V was deposited on the top of the interfacial layer by thermal evaporation at a substrate temperature of 90°C and a deposition rate in the range of 0.4~0.5 Å/s. Then, 5 nm MoO_3 and 50 nm Au were thermally evaporated on the top of the device at room temperature. The channel length (L) and width (W) were 500 μm and 1.5 mm, respectively. We have carried out all of the depositions under the working pressures of below 2×10^{-6} Torr while monitoring the film thickness with a quartz crystal microbalance. To investigate the charge transport mechanism, the device was cooled down using a cryostat. The V_D-I_D characteristic was measured in the temperature range between 133 and 293 K by flowing liquid nitrogen into the vacuum chamber using semiconductor parameter analyzer (HP4155B).

3. Results and Discussions

Figures 2(a) and 2(b) show V_D-I_D characteristics with different V_G in the temperature range between 133 K and 293 K, under forward and reverse V_D condition, respectively. Temperature dependence of V_D-I_D characteristics can be explained with two possible charge transport mechanisms which are Schottky thermionic emission and polycrystalline model at ground boundary. [4] In the forward applied voltage V_D region, temperature dependence of V_D-I_D characteristics can be fitted by the Schottky thermal emission mechanism model with barrier height range from 33 to 57 meV, as shown in Fig. 3. At V_G = 0 V, lower value of 8 meV was observed. This is because current level is much lower than hole with higher energy level was over the barrier height of metal electrode. It is presumably due to barrier height of grain boundary under low current region. On the other hand, in the reverse applied voltage V_D region, temperature dependence of V_D-I_D characteristics can be fitted by the Schottky thermal emission mechanism model with barrier height range from 49 to 73 meV, as shown in Fig. 4. At V_G = 0 V, lowest value of 3 meV was observed. By applying gate voltage, rapid increase of the barrier height was observed and the barrier height was gradually decreased with increase in the negative gate voltage.



(a) Forward V_D condition. (b) Reverse V_D condition.

Fig. 2 Temperature dependence of V_D-I_D characteristics.

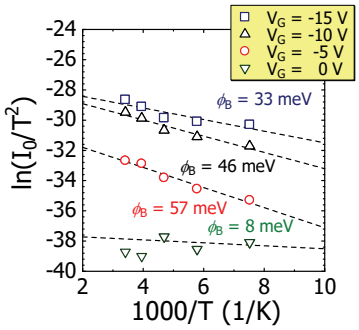


Fig. 3 Relationship between $\ln(I_0/T^2)$ vs 1,000/T characteristics (lower voltage region).

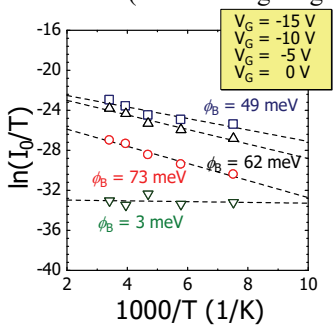


Fig. 4 Relationship between $\ln(I_0/T^2)$ vs 1,000/T characteristics (high voltage region).

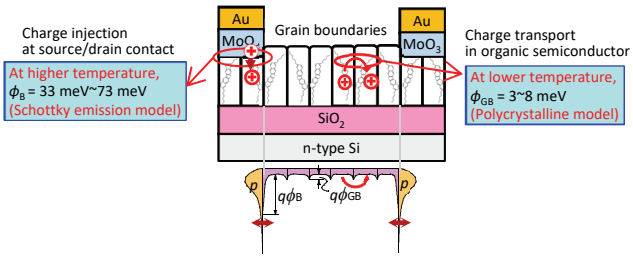


Fig. 5 Possible mechanism of conduction model.

We will consider a conduction model in C6-DNT-V TFTs. Nakamura *et al.* [4] reported that barrier height of 150 meV at grain boundary, band fluctuation in the domain is 30 meV, and charge transport is explained using polycrystalline model in pentacene TFT. The activation energy of the C6-DNT-V between 33 and 73 meV is originate from the Schottky thermal emission between C6-DNT-V and MoO_3/Au electrode, where, typical value of mobility was 1.5 cm^2/Vs with C6-DNT-V thickness of 40 nm. The mobility was decreased to 0.6 cm^2/Vs with only Au electrode and another process condition of C6-DNT-V TFT was not changed, *i.e.*, crystal growth of organic layer is identical. Under low current level at $V_G = 0$, drain current was proportional to the drain voltage and smaller activation energy of 8 and 3 meV were obtained. Figure 5 shows possible mechanism of conduction model. For smaller gate voltage, the drain current was proportional to the drain voltage [4], as shown in Fig. 2. Equation of the polycrystalline model is as follows: [4]

$$J = qn_h\mu_h\sqrt{\frac{qN_A\phi_{GB}}{2\varepsilon_s}}\,exp\left(-\frac{q\phi_{GB}}{k_BT}\right)\frac{qV_b}{2k_BT}, \quad (1)$$

where, q is the unit charge, μ_h is the mobility in the domain, N_A is the carrier concentration, ε_S is the dielectric constant, k_B is the Boltzmann constant, T is the temperature, ϕ_{GB} is the barrier height at grain boundary and V_b equals $V_D/(L/\ell)$, L is the channel length, and ℓ is the grain size.

This lowness of activation energy is due to the conduction of C6-DNT-V thin films, where, the stacking structure of π-conjugated core is much closer and grain boundary is much less than that of pentacene thin films. [2, 5]

4. Conclusions

We have investigated gate-bias and temperature dependence in C6-DNT-V TFTs with MoO_3/Au electrodes. Two possible conduction mechanism and lower activation energy were observed related to the tightly stacked structure of organic molecule. Evaluation of the temperature dependence in the OTFT is interesting to study the conduction mechanism of the organic thin films.

Acknowledgements

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