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Influence of Surface Treatment of SiO_2 Gate Insulator for Pentacene-based OFETs with Nitrogen-doped LaB_6 Bottom-Contact Electrode Formation Process

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Abstract

In this paper, surface treatment of SiO_2 gate insulator after the photolithography process of bottom contact electrode formation for pentacene-based organic field-effect transistor (OFET) was investigated. It was found that mobility was improved from $2.8x10^{-3}$ to 0.11 $cm^2/(Vs)$ by SPM and DHF surface treatment process and nitrogen-doped LaB_6 interfacial layer. Furthermore, steep subthreshold swing of 78 mV/dec. was achieved for the fabricated OFETs with top-contact electrode geometry.

1. Introduction

Organic field-effect transistors (OFETs) have attracted much attention because of their unique properties such as flexible and light weight although the mobility is worse compared to that of Si. Furthermore, some organic materials are available for spincoating, inkjet printing, and imprinting method. Pentacene is well known as p-type organic semiconductor, and its high hole mobility such as 1 $cm^2/(Vs)$ was reported [1]. We have investigated pentacene-based CMOS utilizing nitrogen-doped (N-doped) LaB_6 interfacial layer (IL) which has a low work function of 2.4 eV and oxidation immunity [2, 3]. We have demonstrated steep subthreshold swing (SS) of pentacene-based p-type OFETs with N-doped LaB_6 IL [4, 5]. However, the degradation of pentacene film quality due to photolithography process must be solved for bottom contact electrode of CMOS. So, in this paper, surface treatment for N-doped LaB_6 patterning process was investigated to improve the interface property of OFETs.

2. Experimental Procedure

The back-gate/bottom-contact pentacene-based OFETs were fabricated with the process flow shown in Fig. 1. Heavily doped n^+-Si(100) substrates were cleaned by SPM (H_2SO_4:H_2O_2 = 4:1) and DHF (HF:H_2O = 1:100). Then, 10-nm-thick SiO_2 was formed on the substrate as a gate insulator by wet oxidation at 850°C. Then, 20-nm-thick N-doped LaB_6 was deposited by RF sputtering with an RF power of 50 W at room temperature (RT), and this film was etched by diluted nitric acid (HNO_3:H_2O = 1:1) by using photolithography process. After that, SPM and DHF treatments were carried out at RT for 15 s, respectively. Next, 1.2-nm-thick N-doped LaB_6 IL was deposited with an RF power of 20 W [4]. Then, 10-nm-thick pentacene (99%, Aldrich) film was deposited without any purification by using thermal evaporation at 100°C with deposition rate of 0.3 nm/min. Finally, Au top contact electrode and Al back gate electrode for OFET were formed by thermal evaporation (L/W = 95 μm/1040 μm). The fabricated OFET was evaluated by I_D-V_G measurement by Agilent 4156C, and pentacene film was evaluated by optical microscopy and X-ray diffraction (XRD).

3. Results and Discussion

Figure 2 shows surface morphology of 10-nm-thick pentacene film. After photolithography process and SPM treatment, the surface of pentacene became rough with island growth as shown in Figs. 2(a) and 2(b). On the other hand, SPM and DHF treatment realized flat surface and N-doped LaB_6 IL made pentacene grains larger. XRD pattern shown in Fig. 3 also confirmed that the surface treatment improved crystallinity of pentacene.

Figure 4 shows the effect of surface treatment on device characteristics. Furthermore, Table 1 lists device parameters of the fabricated OFETs for comparison. The OFETs worked when N-doped LaB_6 IL was introduced even without surface treatment. In addition, steep subthreshold swing was realized. As shown in Table 1, it was found that surface treatment led to improve the mobility to 0.11 $cm^2/(Vs)$ and hysteresis width, and N-doped LaB_6 IL can realize negative V_{TH} shift and steep SS of 78 mV/dec.

4. Conclusion

In this paper, surface treatment for N-doped LaB_6 patterning process was investigated. It was found that SPM and DHF treatments at room temperature improved mobility and N-doped LaB_6 IL realized steep SS. As a conclusion, these processes are necessary for pentacene-based CMOS fabrication with N-doped LaB_6 bottom contact electrode to realize high mobility and steep subthreshold characteristic of OFETs.

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Reference

[1] S. Lee, *et al.*, Appl. Phys. Lett., **88**, 162109 (2006). [2] H. Ishii, *et al.*, ECS Trans., **66**, 41, pp. 23–28 (2015). [3] Y. Maeda, *et al.*, IEICE Trans. Electron., **E99-C**, pp. 535–540 (2016). [4] Y. Maeda, *et al.*, Jpn. J. Appl. Phys., **56**, 04CL06 (2017). [5] Y. Maeda, *et al.*, IEICE Trans. Electron., **E100-C**, pp. 463–467 (2017).

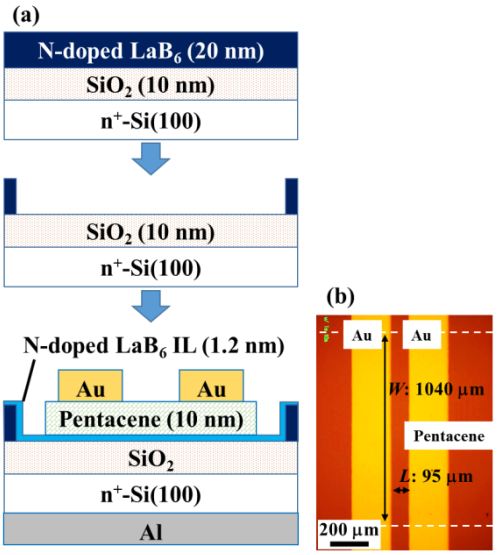

Figure 1 (a) Experimental procedure and (b) top view of the fabricated OFET.

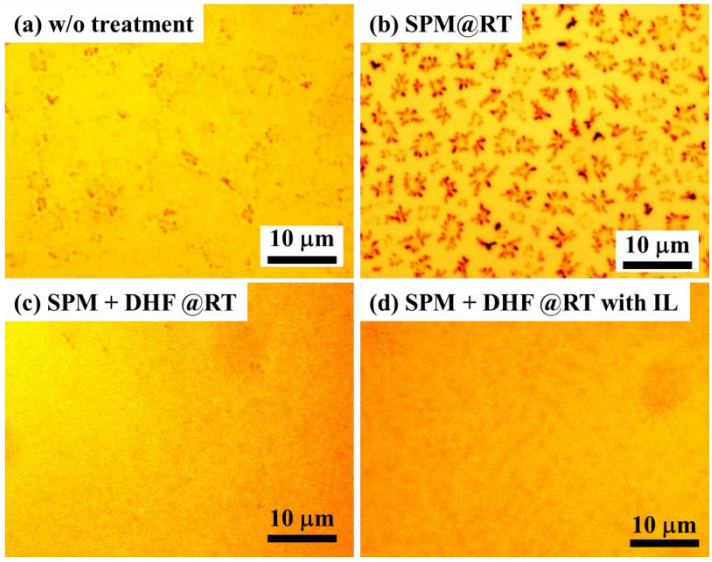

Figure 2 Surface morphology of 10-nm-thick pentacene film. (a) W/o treatment, (b) with SPM treatment, (c) with SPM and DHF treatment and (d) with N-doped LaB_6 IL after SPM and DHF treatment.

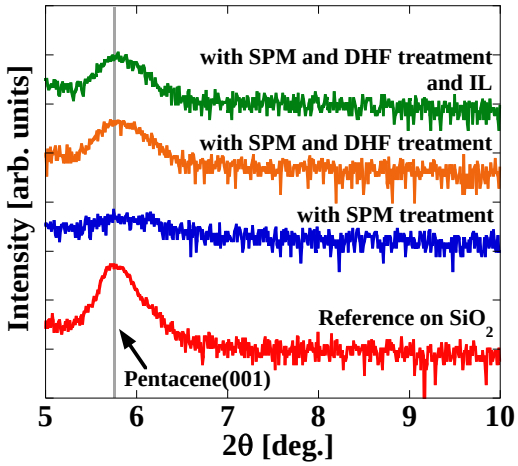

Figure 3 XRD pattern of 50-nm-thick pentacene film.

Table 1 Device parameters of the fabricated OFETs.

Surface treatment	N-doped LaB_6 IL	μ [cm^2/(Vs)]	V_{TH} [V]	SS [mV/dec.]	Hysteresis width [V]
as-formed [4]	w/o	0.25	5.5	350	0.37
as-formed [4]	with	0.26	-1.0	75	0.078
w/o	with	2.8×10^{-3}	-0.85	97	1.3
with	with	0.11	-0.71	78	0.20

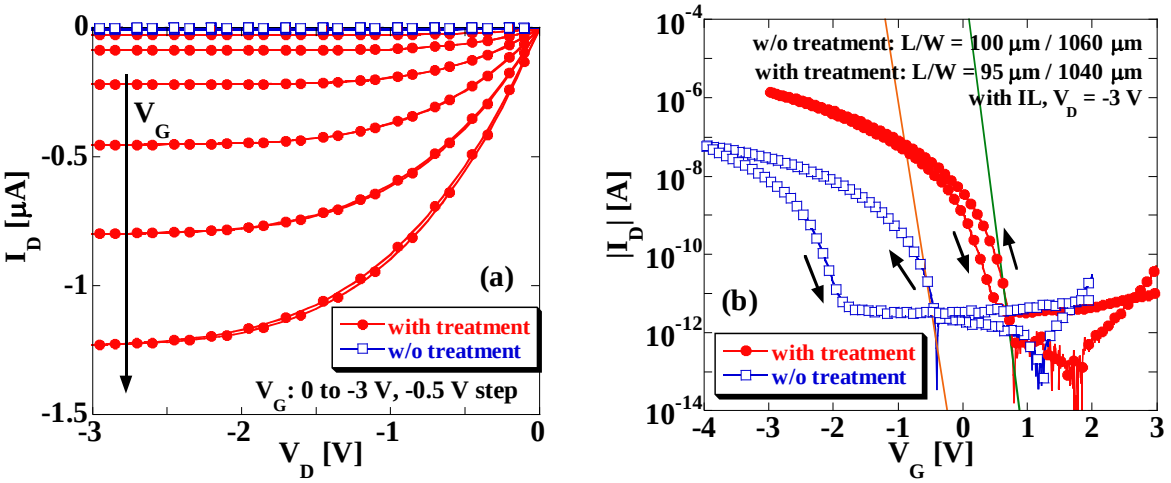

Figure 4 Effect of surface treatment on (a) I_D-V_D and (b) I_D-V_G characteristics.