Carrier Transport across ITO/MoO_x/SiO_x/Si Interfaces

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Abstract

Carrier selective contact (CSC) cells sometimes show "S"-shaped current-voltage (I-V) curves and the cell performances are lower than as expected. In this work, a mechanism of "S"-shape was studied for an ITO/MoO_x/SiO_x/n-cSi cell from the viewpoint of the I-V characteristics across the ITO/MoO_x/SiO_x/Si interfaces. To experimentally simulate the effect of hole-inversion layer/n-cSi diode property, a test cell device using a p-type substrate was fabricated (ITO/MoO_x/SiO_x/p-cSi). By high-temperature forming-gas annealing, the I-V curves of this device changed from linear to non-linear. As a whole, this trend well explained the "S"-shape enhancement. The ITO/MoO_x/SiO_x/hole-inversion layer can be equivalently regarded as an n-p diode with a parallel conductance. In the presentation, the relation between these I-V properties and the MoO_x/SiO_x/Si interface properties with respect to defect densities and band alignment will be also discussed.

1. Introduction

Carrier-selective contact (CSC) cells are expected as next generation high-efficient Si heterojunction cells with low cost. In an n-type substrate CSC, transition-metal oxides (TMOs), such as MoO_x and VO_x are widely studied as hole-selective contact materials [1, 2]. The carrier transport through the TMO/SiO_x/n-cSi layers and the formation of hole inversion layer at the Si surface determine the solar cell performance, such as fill factor (FF) and open-circuit voltage (V_{OC}).

In CSC cell properties, a so-called "S-shape" characteristic often appears in the current-voltage (I-V) curve. Since the mostly used TMOs are degenerated n-type semiconductors, the TMO/SiO_x/n-cSi forms an n-n structure. Thus, if conduction band energy of the TMO is not higher than that of hole Fermi-level at the n-cSi surface [3], holes in the inversion layer at the n-cSi surface cannot transport into the n-type TMO, leading to no current flow. In actual, however, many CSC devices operate as solar cells. These facts indicate that some carrier transport paths via defects by carrier recombination are formed at TMO/SiO_x/Si interfaces [4].

So far, several earlier works have reported on the possible factors related to the "S"-shape phenomena, such as ITO/MoO_x interface property [5], MoO_x thickness and defect [6]. However, no direct evidence was shown and the mechanism is still unclear. It is required to understand in

detail the device physics to improve the performance of cells using n-type TMO materials with n-cSi.

In this work, the relation between the I-V properties of $ITO/MoO_x/SiO_x/hole-inversion$ layer structure and the "S"-shaped characteristics in the $ITO/MoO_x/SiO_x/n-cSi$ cell was studied. To experimentally simulate the effect of hole-inversion layer/n-cSi diode property, a complemental test structure cell was fabricated using a p-type Si substrate (i.e. $ITO/MoO_x/SiO_x/p-cSi$), as well as an n-type cell. The light-illuminated and dark I-V curves were obtained for different forming-gas annealing temperatures to change the properties of involved interfaces. The mechanism of the "S"-shape characteristics is discussed with possible hole conductance paths.

2. Experimental

An ITO/MoO_x/SiO_x/n-cSi contact cell [Fig. 1(a)] was fabricated as follows. A Cz n-type crystalline Si(100) wafer was used as a substrate. The substrate was chemically cleaned and oxidized in a hot nitrogen-acid (HNO₃) at 80 °C for 10 min to grow SiO_x layer around 1.8 nm. A MoO_x layer was then deposited on the SiO_x layer by thermal evaporation about 30-nm-thick. An ITO film was then deposited by reactive-plasma deposition for about 50-nm-thick. An Al electrode was thermally evaporated onto the rear surface with the SiO_x to form an electron selective contact with the substrate.

An alternative front junction test cell (ITO/MoO_x/SiO_x/p-cSi) device was fabricated [Fig. 1(b)] by applying the same process as the n-type cell but an Al back electrode on the rear surface without SiO_x on it.

The cell devices were annealed in a forming gas ambient (4% H_2 in N_2) at from 200 to 300 °C for 15 min. The current-voltage (I-V) curves were obtained under a light illumination with AM 1.5 or a dark condition.



Fig. 1 Fabricated device structures: $ITO/MoO_x/SiO_x$ contact cells using (a) n-type and (b) p-type substrates.

3. Results and Discussion

The light-illuminated I-V curves of the ITO/MoO_x/SiO_x/n-cSi cells (n-type cells) were shown in Fig. 2 (a) for different annealing temperatures. For as-deposition and 200 °C, the I-V curves exhibited almost no "S"-shape. After high temperature annealing at equal to and more than 250 °C, I-V curves were distorted and the "S"-shape becomes prominent.

The light-illuminated I-V curves for the ITO/MoO_x/SiO_x/p-cSi cells were shown in Fig. 2(b). Almost linear relation was obtained for as-deposition condition. After high temperature annealing at equal to and more than 200 °C, the curves showed non-linear relations. The non-linearity was enhanced as the temperature increased. As a whole, this trend is agreed with the n-cells although a slight discrepancy is seen in the data for 200 °C. The present results experimentally demonstrate that the "S"-shape of the n-cell is mainly attributed to the properties of the ITO/MoO_x/SiO_x/hole-inversion layer.



Fig. 2 Light-illuminated I-V curves of (a) $ITO/MoO_x/SiO_x/n-cSi/SiO_x/Al$ and (b) ITO/MoO/SiO/p-cSi/Al cells.

The I-V curves under the dark condition were also obtained, as shown in Fig. 3. Qualitatively, these curves can be understood as an n-p diode behavior with a parallel conductance. The magnitude of parallel conductance is considered to the size of the carrier transport path through the $MoO_x/SiO_x/Si$ interfaces. Assuming the above simplest equivalent circuit model, the conductance can be estimated from the slope of the curve at zero volt. The values of conductance are about 0.003 and 0.001 S for as-deposition and 200 °C, respectively. At 250 and 300 °C, the conductance decreases by an order of magnitude, estimated about 3 μ S. These conductance changes might correspond to the amount of defects associated to the carrier transport from the hole-inversion to MoO_x layer. In the presentation, the relation between these I-V properties and the MoO_x/SiO_x/Si interface properties such as defect density and band alignment will be also discussed.



Fig. 3 Annealing temperature dependence of dark I-V curves of ITO/MoO_x/SiO_x/p-cSi/SiO_x/Al cells.

3. Conclusions

"S"-shape The characteristics appeared in an ITO/MoO_x/SiO_x/n-cSi contact cell is mainly caused by the n-p diode behavior of the ITO/MoO_x/SiO_x/hole-inversion layer structures. This structure can be regarded as an equivalent n-p diode circuit with a parallel conductance. The "S"-shape is enhanced by reducing the conductance, suggesting that the carrier transport path from the hole-inversion to MoO_x layers is shrunk. The relation between these I-V properties and the MoO_x/SiO_x/Si interface properties with respect to defect densities and band alignment will be also discussed in the presentation.

Acknowledgements

This work was partly supported by NEDO, METI (Japan).

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