Integration of Photonics with Digital Processing Units

Luca Alloatti

1Institute of Electromagnetic Fields (IEF), ETH Zurich, Zurich, Switzerland
Phone: +41 44 632 78 26, E-mail: luca.alloatti@ief.ee.ethz.ch

Abstract

The performance of modern computer systems is limited by the input/output (I/O) bottleneck caused short-reach electrical interconnects. Monolithic integration of photonics and electronics has the potential of solving this problem. Key figures-of-merit are discussed, and a complete 12.5 GBd photonics toolbox is presented in a 45 nm node.

1. Introduction

While the minimum feature size of semiconductor technology nodes keeps shrinking, most Digital Processing Units (DPUs) are increasingly limited by the input/output (I/O) bottleneck of existing electrical wirelines, [1]. An illustration of this trend is given by the Graphics Processing Units (GPUs) of NVIDIA, Fig. 1. Such devices are currently used not only for graphics, but also for general-purpose (GP) computation. In the GP context, a safe rule-of-thumb requires that for every floating-point-operation (FLOP) there is one byte (B) of I/O, [2]. Unfortunately, while this condition was met for GPUs around 2007, Fig. 1, the gap has increased since, and it is expected to worsen because of the limited performance of electrical interconnects, [3].

However, most silicon photonics research is today targeting datacom and telecom applications [4]–[7] where the required energy efficiencies and bandwidth densities are orders-of-magnitude smaller than for chip-to-chip computer applications.

Historically, the development of silicon foundries for electronics and for photonics have followed different paths because of a number of conflicting requirements. For example, electronic circuits generally benefit from the shrinking of the transistors’ dimensions, while optical waveguides instead must have a cross-section in the order of the effective wavelength of light. Most importantly, moreover, photonics requires a material for photodetection. As a consequence, most silicon photonics foundries have been modified such as to incorporate pure germanium in their process flows -a material which is generally absent in electronics foundries.

2. Zero-Change CMOS Photonics

A different approach as been proposed by Orcutt et al. in 2011, [8]. This approach consists of utilizing existing electronics CMOS foundries and of adapting the photonics to the foundry rather than the other way around. In particular, within the zero-change approach, no critical Design Rule (DR) can be violated, nor new materials can be added. Since electronics foundries were developed keeping transistors in mind, the “zero-change” approach required solving several design and physical challenges.

The design challenges were circumvented by manhattanizing all the shapes (e.g. microrings) on a fine-grained orthogonal grid, [9], and by the automatic removal of DR violations within a novel Photonic Design Automation (PDA) tool, Fig. 3, [10].
The novel PDA tool enabled to rapidly optimize all the photonics components [10]. The toolbox currently comprises a low-voltage 13 GHz modulator, [12], a resonance-enhanced 12.5 Gb/s photodiode with 58% quantum efficiency Fig. 4, [13], and vertically-illuminated photodiodes for packaging chips on optical-circuit-boards (OCBs), [14]. The improved performance of these devices is expected to increase the wall-plug energy efficiency beyond 1 b/bit and the bandwidth density up to 10 Tb/s/mm², Fig. 2, [15]. The strict enforcement of the DRs and the high material quality of advanced CMOS nodes lead to beneficial effects such as low photodiode dark currents and the reproducibility of the device performance.

4. Conclusions
A complete photonics toolbox in an unmodified 45 nm process was demonstrated. These results show not only that electronics and photonics process flows can be compatible, but also that apparent limitations enforced by the electrical design and fabrication flows can be beneficial to photonics.

References