Extended Abstracts of the 2017 International Conference on Solid State Devices and Materials, Sendai, 2017, pp143-144

C-5-01 (Invited)

Integration of Photonics with Digital Processing Units

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Invited

Abstract

The performance of modern computer systems is limited by the input/output (I/O) bottleneck caused short-reach electrical interconnects. Monolithic integration of photonics and electronics has the potential of solving this problem. Key figures-of-merit are discussed, and a complete 12.5 GBd photonics toolbox is presented in a 45 nm node.

1. Introduction

While the minimum feature size of semiconductor technology nodes keeps shrinking, most Digital Processing Units (DPUs) are increasingly limited by the input/output (I/O) bottleneck of existing electrical wirelines, [1]. An illustration of this trend is given by the Graphics Processing Units (GPUs) of NVIDIA, Fig. 1. Such devices are currently used not only for graphics, but also for general-purpose (GP) computation. In the GP context, a safe rule-of-thumb requires that for every floating-point-operation (FLOP) there is one byte (B) of I/O, [2]. Unfortunately, while this condition was met for GPUs around 2007, Fig. 1, the gap has increased since, and it is expected to worsen because of the limited performance of electrical interconnects, [3].

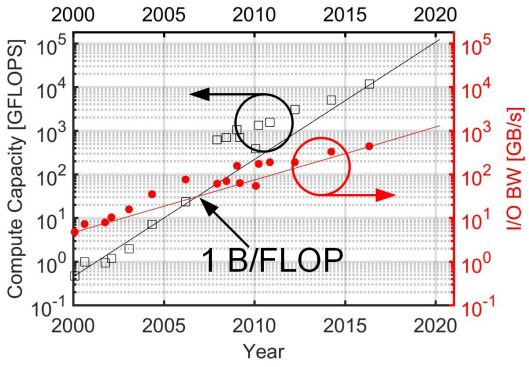

Fig. 1 | Evolution of single-precision floating-point compute capacity (black squares) and of the I/O bandwidth (red dots) of NVIDIA GPUs.

If the trend shown in Fig. 1 is conserved, single-chip microprocessors will reach by year 2021 a performance of 125 TFLOPS which would require and I/O bandwidth of 10^{15} b/s (1 Pb/s) for satisfying the 1 B/FLOP condition. Assuming a power budget of 100 W and a chip surface of 100 mm^2 for the I/O only, this value corresponds to an energy efficiency of 10 b/pJ and a bandwidth density of 10 Tb/s/mm^2, Fig. 2.

However, most silicon photonics research is today targeting datacom and telecom applications [4]–[7] where the required energy efficiencies and bandwidth densities are orders-of-magnitude smaller than for chip-to-chip computercom applications.

Historically, the development of silicon foundries for electronics and for photonics have followed different paths because of a number of conflicting requirements. For example, electronic circuits generally benefit from the shrinking of the transistors' dimensions, while optical waveguides instead must have a cross-section in the order of the effective wavelength of light. Most importantly, moreover, photonics requires a material for photodetection. As a consequence, most silicon photonics foundries have been modified such as to incorporate pure germanium in their process flows -a material which is generally absent in electronics foundries.

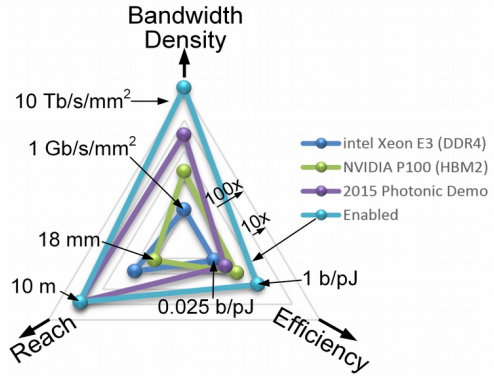

Fig. 2 | Radar chart of the I/O performance of state-of-the-art electronic and photonic links (legend). The scale is logarithmic and every line corresponds to a factor of ten.

2. Zero-Change CMOS Photonics

A different approach as been proposed by Orcutt et al. in 2011, [8]. This approach consists of utilizing existing electronics CMOS foundries and of adapting the photonics to the foundry rather than the other way around. In particular, within the zero-change approach, no critical Design Rule (DR) can be violated, nor new materials can be added. Since electronics foundries were developed keeping transistors in mind, the "zero-change" approach required solving several design and physical challenges.

The design challenges were circumvented by manhattanizing all the shapes (e.g. microrings) on a fine-grained orthogonal grid, [9], and by the automatic removal of DR violations within a novel Photonic Design Automation (PDA) tool, Fig. 3, [10].

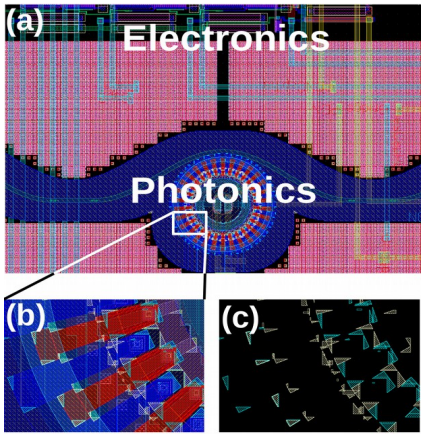

Fig. 3 | Design-Rule (DR) cleaning of a layout. (a) Electronic and photonic circuits are designed side-by-side with the same CAD tool. (b) Details of the microring resonator implant masks. (c) Same region as (b) showing the shapes which have been added/removed automatically by the DR-cleaning algorithm.

From a physical perspective instead, zero-change modulators and waveguides could be fabricated in a number of different nodes. In the 45 nm SOI node of GlobalFoundries, the photonics toolbox could be completed by adding a photodiode. The photodiode exploits carrier generation in the silicon-germanium (SiGe) which is present in the process for stressing the channel of p-FETs. Because of the low germanium content of the SiGe alloy, the wavelength had to be moved closer to the bandgap of silicon, [11]. The first photodiode had a quantum efficiency of few percent and enabled in 2015 the realization of the first microprocessor with optical I/O, [1], [11]. However, the total energy efficiency was not yet competitive with electrical wirelines, Fig. 2.

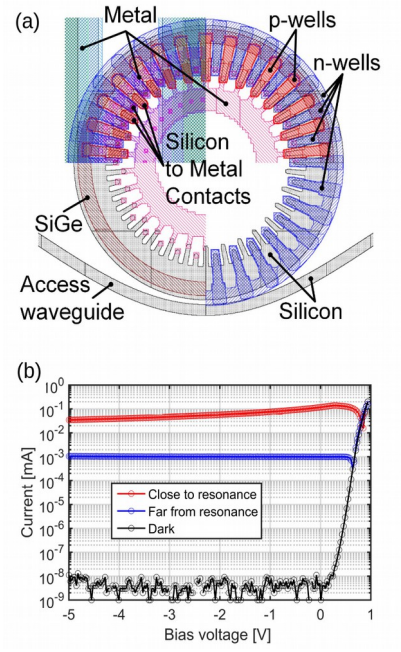

Fig. 4 | Resonance-enhanced photodiode. (a) The layout consists of a ring-resonator including a SiGe ring and T-shaped implants. (b) Illuminated and dark-current vs. bias voltage.

The novel PDA tool enabled to rapidly optimize all the photonics components [10]. The toolbox currently comprises a low-voltage 13 GHz modulator, [12], a resonance-enhanced 12.5 GBd photodiode with 58 % quantum efficiency Fig. 4, [13], and vertically-illuminated photodiodes for packaging chips on optical-circuit-boards (OCBs), [14]. The improved performance of these devices is expected to increase the wall-plug energy efficiency beyond 1 b/bit and the bandwidth density up to 10 Tb/s/mm^2, Fig. 2, [15]. The strict enforcement of the DRs and the high material quality of advanced CMOS nodes lead to beneficial effects such as low photodiode dark currents and the reproducibility of the device performance.

4. Conclusions

A complete photonics toolbox in an unmodified 45 nm process was demonstrated. These results shows not only that electronics and photonics process flows can be compatible, but also that apparent limitations enforced by the electrical design and fabrication flows can be beneficial to photonics.

References

[1] C. Sun *et al.*, "Single-chip microprocessor that communicates directly using light," *Nature*, vol. 528, no. 7583, pp. 534–538, 2015.

[2] S. Williams, A. Waterman, and D. Patterson, "Roofline: An Insightful Visual Performance Model for Multicore Architectures," *Commun ACM*, vol. 52, no. 4, pp. 65–76, 2009.

[3] D. Friedman, "ISSCC 2016 Trends, Wireline," 2016.

[4] R. Blum, "Intel Silicon Photonics Enabling Data Center Connectivity," *OFC 2016 Intel*, 2016.

[5] F. Boeuf, J. F. Carpentier, C. Baudot, P. Le Maitre, and J.-R. Manouvrier, "Silicon Photonics Research and Manufacturing Using a 300-mm Wafer Platform," in *Silicon Photonics III: Systems and Applications*, L. Pavesi and J. D. Lockwood, Eds. Berlin, Heidelberg: Springer Berlin Heidelberg, 2016, pp. 277–315.

[6] S. Meister *et al.*, "Silicon photonics for 100 Gbit/s intra-data center optical interconnects," *Proc SPIE*, vol. 9753, pp. 975308-975308–7, 2016.

[7] J. Orcutt *et al.*, "Monolithic Silicon Photonics at 25Gb/s," in *OFC 2016*, 2016, p. Th4H.1.

[8] J. S. Orcutt *et al.*, "Nanophotonic integration in state-of-the-art CMOS foundries," *Opt. Express*, vol. 19, no. 3, pp. 2335–2346, Jan. 2011.

[9] J. S. Orcutt and R. J. Ram, "Photonic Device Layout Within the Foundry CMOS Design Environment," *IEEE Photonics Technol. Lett.*, vol. 22, no. 8, pp. 544–546, Apr. 2010.

[10] L. Alloatti, M. Wade, V. Stojanovic, M. Popovic, and R. J. Ram, "Photonics design tool for advanced CMOS nodes," *IET Optoelectron.*, vol. 9, no. 4, pp. 163–167, 2015.

[11] L. Alloatti, S. A. Srinivasan, J. S. Orcutt, and R. J. Ram, "Waveguide-coupled detector in zero-change complementary metal-oxide-semiconductor," *Appl. Phys. Lett.*, vol. 107, no. 4, p. 41104, 2015.

[12] L. Alloatti, D. Cheian, and R. J. Ram, "High-speed modulator with interleaved junctions in zero-change CMOS photonics," *Appl. Phys. Lett.*, vol. 108, no. 13, 2016.

[13] L. Alloatti and R. J. Ram, "Resonance-enhanced waveguide-coupled silicon-germanium detector," *Appl. Phys. Lett.*, vol. 108, no. 7, p. 71105, 2016.

[14] L. Alloatti and R. J. Ram, "Infrared vertically-illuminated photodiode for chip alignment feedback," *AIP Adv.*, vol. 6, no. 8, p. 85219, 2016.

[15] L. Alloatti, "High-Speed Photonics for Side-by-Side Integration with Billion Transistor Circuits in Unmodified CMOS Processes," *J. Light. Technol.*, vol. PP, pp. 1–1, 2017.