

High-Performance Surface Illumination-type Ge Photodetector for Optical Interconnection on 300mm-diameter of SOI substrate

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Abstract

We studied a high speed and high efficiency of vertically-illuminated p-i-n Ge photodetector (Ge-PD) with Ge thickness of around 500 nm and 1800 nm. In case of 500 nm thick Ge layer, we proposed the Ge-PD of the concentric p-i-n electrode structure of Si under the Ge mesa. In case of 1800 nm thick Ge layer, we developed a vertical p-i-n structure of Ge-PD and demonstrated high-responsivity of 0.8-0.9 A/W and high-speed of 25 Gbps at 1.3 μm wavelength.

1. Introduction

Silicon photonics has recently attracted much attention because it offers low cost, low power consumption, and high bandwidth for optoelectronic solutions for applications ranging from telecommunications to chip-to-chip interconnects [1]. To realize an effective photonics-electronics convergence system, it is very important to achieve a high-speed and high-efficiency Ge-PD.

In addition, in order to achieve a high optical-coupling efficiency with a multimode optical fiber, a vertically-illuminated Ge-PD is promising [2,3]. However, there has been trade-off relationship between bandwidth and efficiency. Therefore, design of a vertically-illuminated Ge-PD structure which satisfy high efficiency and high speed is very important to achieve high bandwidth and low power optical interconnect. In addition, it is necessary to thin the height of Ge-PD for Si photonics circuit integration to realize multilayer metal wiring.

In this paper, we study a high-speed and high-efficiency of Ge-PD with 500 nm thick and 1800 nm thick Ge layers. In case of a 500 nm-thick Ge layer, we propose the Si-based lateral p-i-n junction electrode with a concentric ring structure under the Ge layer, and demonstrate low electrical capacitance and 0.5 A/W of responsivity. In case of 1800 nm-thick Ge layer, we demonstrate high-responsivity of 0.8-0.9 A/W and high-speed of 25 Gbps at 1.3 μm wavelength.

2. Experiment and Results

2-1 Concentric ring shape electrode structure for 500 nm-thick Ge-PD

Figure 1 shows (a) schematic cross-section of Ge-PD with lateral Si-pin junction and (b) horizontal image of Si-pin junction for bottom electrode under the Ge layer. In case of 500 nm-thick Ge layer, we study the Ge-PD which consists of i-Ge layer on a concentric ring-shape p-i-n junction electrode of a SOI (silicon-on-insulator) substrate. The fabrication process started from a 300 mm-diameter SOI wafer, of which SOI thickness was 200 nm. A Si pedestal was patterned by immersion ArF lithography and dry etching. Then, boron and phosphorus ions were implanted and

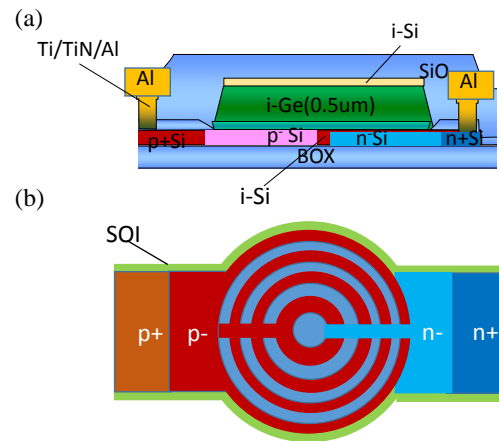


Fig. 1: (a) Schematic cross-section of Ge-PD with lateral Si-pin junction and (b) horizontal image of Si-based lateral-pin junction for bottom electrode under the Ge layer.

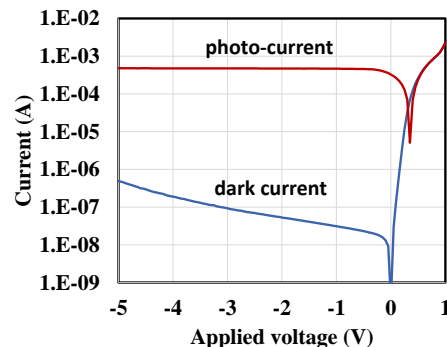


Fig. 2: I-V characteristics of Ge-PD with a concentric ring Si pin junction electrode with and without input light.

the wafers were annealed to form a concentric ring-shape of p-Si and n-Si for the bottom electrode. Then a 500 nm-thick epitaxial germanium mesa were selectively grown on the Si pedestal by reduced-pressure chemical vapor deposition (RPCVD) method. A 30 nm-thick Si-capping layer was also deposited on a Ge layer to passivate the Ge surface. Then a SiO₂ upper-clad layer was deposited, and contact-holes were formed by UV lithography and dry-etching process. Finally, metal electrodes of Ti/TiN/Al layers were deposited and patterned. Figure 2 shows I-V characteristics of the Ge-PD. Photo-responsivity of 0.5 A/W was obtained with low dark current of 100 nA at -3 V_{dc}. From the S-parameter analysis, low electrical capacitance of 30 fF was confirmed.

In this structure, the distance between p and n-type electrodes affects the photo-carrier transit time. In addition, the additional resistance depends on their widths. By optimiz-

ing the widths of p and n-type concentric ring-shape electrodes, over 10 GHz bandwidth could be obtained from T-CAD simulation.

2-2 Vertical p-i-n structure for 1800nm-thick Ge-PD

Figure 3 shows (a) a schematic diagram surface-illumination type Ge-PD and (b) SEM images of fabricated device. The fabrication process started from a 300 mm-diameter SOI wafer, of which SOI thickness was 180 nm. A Si pedestal was patterned by immersion ArF lithography and dry etching. Then, B ions were implanted and the wafers were annealed to form p⁺-Si of the bottom electrode. The 1800 nm-thick epitaxial germanium mesas were selectively grown on the Si pedestal by RPCVD. A 25 nm-thick Si capping layer was deposited on a Ge layer to passivate the Ge surface and P ion implantation was performed. Then a SiO₂ upper-clad layer was deposited, and contact-holes were formed by UV lithography and dry-etching process. Next, metal electrodes of Ti/TiN/Al layers were deposited and patterned. Then, SiN_x/SiO₂ multi-stacked layers were deposited as anti-reflection coating. In this study, Cu/polyimide layers were stacked on the first clad layer to flatten the wafer surface with 1800nm-thick Ge layer to form the 2nd electrical wiring, which contributed to low RF loss of electrical wiring and bandwidth for the optical receiver chip [4].

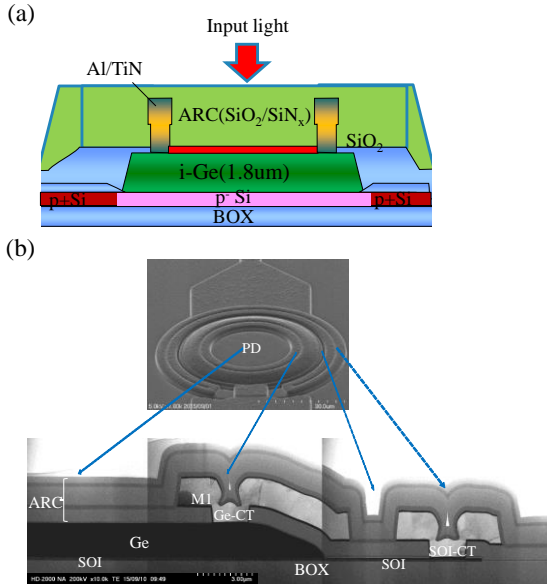


Fig. 3: (a) Schematic diagram of surface-type Ge photodiode and (b) SEM images of fabricated device.

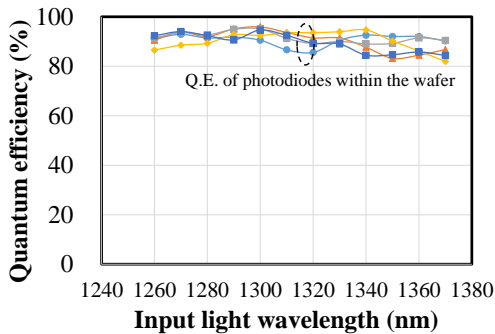


Fig. 4 Quantum efficiency dependence on input light wavelength for Ge-PD within the wafer.

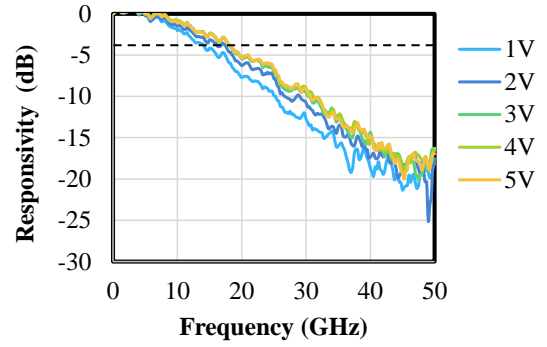


Fig. 5: Frequency response of Ge-PD dependence on V_{dc}.

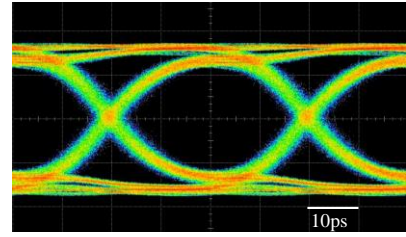


Fig. 6: Output waveform at 25 Gbps with 2⁷-1 PRBS at 1.3 μm wavelength from optical receiver chip.

Figure 4 shows quantum efficiency dependence on input light wavelength for the Ge-PD within the wafer. By optimizing the anti-reflection coating stack structure, high responsivity of 0.8-0.9 A/W was uniformly obtained within the wafer.

Figure 5 shows frequency response of the Ge-PD dependence on V_{dc} in case of 25 μm-diameter. At 3 V_{dc}, about 15 GHz bandwidth was obtained. In case of the Ge-PD with thick Ge-layer, photo-carrier transit time mainly limits the frequency bandwidth. Therefore, we optimized the layered structure of Ge thickness on SOI to satisfy the high-responsivity and high-bandwidth.

Figure 6 shows an output waveform from integrated CMOS-TIA (trans-impedance amplifier) at 25 Gbps with 2⁷-1 PRBS at 1.3 μm wavelength at 3.3 V_{dc}. Clear eye opening was obtained, which would contribute to the efficient optical interconnect [5].

4. Conclusions

We studied a high-speed and high-efficiency of Ge-PD with 500 nm-thick and 1800 nm-thick Ge layers. In case of a 500 nm-thick Ge layer, we propose the Si-based lateral p-i-n junction electrode with a concentric ring structure, and demonstrated low electric capacitance and 0.5 A/W of responsivity. In case of 1800 nm-thick Ge layer, we demonstrated high-responsivity of 0.8-0.9 A/W and high-speed of 25 Gbps at 1.3 μm wavelength.

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