Extended Abstracts of the 2017 International Conference on Solid State Devices and Materials, Sendai, 2017, pp169-170

D-1-01 (Invited)

SSDM2017
Physical modeling of carbon nanotube based nanoelectromechanical memory cell SET and RESET operations

M. Stopa and T. Rueckes
Nantero Corporation, Inc.
25E Olympia Ave., Woburn, MA 01801, USA
Phone: +1-508-207-6697 E-mail: mstopa@nantero.com

Abstract

We employ a continuum quasi-elastic mechanical model along with a circuit description for the charge accumulation in a non-equilibrium current-carrying state of transport between metal electrodes and through the carbon nanotube (CNT) medium of an NRAM® (Nano Random Access Memory) cell. We determine the voltage dependent strain and, self-consistently, the inhomogeneous tunnel resistivity of the CNT material, treating transport in the latter as a network of tunnel couplings. Thus, the nonlinear I-V characteristics of the device are computed.

1. Introduction

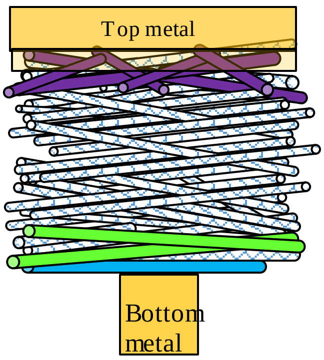

Figure 1 Illustration of NRAM, CNT memory cell. Switching layer (green CNT region) close to bottom lead.

The NRAM memory cell (Fig. 1, [1-3]) consists of top and bottom metal electrodes, typically made from TiN, and a region of roughly 40 nm thickness of carbon nanotube materials. A variety of CNT materials – for example partially ordered or "rafted," or else disordered and also of varying CNT diameters – are laid down via spin coating with the CNTs extending principally in the plane of the device. The overall circular structure (the diameter of which varies but in this publication we take d=540 nm) therefore conducts electrons vertically through a succession of tunnel junctions between CNTs and between the electrodes and the neighboring CNTs.

The state of the memory bit is manifested in its resistance: either a low resistance "SET" state or a high resistance "RESET" state. Switching between these states, is achieved by all electrical pulsing of varying strengths and polarities. We understand the two states to differ in the numbers and strengths of their tunnel connections from top to bottom and thus the switching is electromechanical in nature.

2. Device operation

Figure 2 illustrates the voltage switching of the memory cell. During this first voltage sweep of the "virgin" material, the resistance decreases with voltage as connections between the CNTs increase in number. At a critical point the resistance jumps, or RESETs, to a higher value (typically above a megaohm). Subsequent pulses of voltage can switch the state repeatedly between SET and RESET.

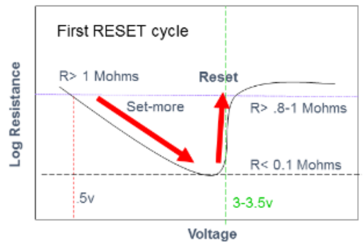

Figure 2 Schematic resistance versus voltage characteristic for first RESET process. Virgin material starts at large (>1 M-ohm) resistance, proceeds to "SET-more" and then abruptly switch back to higher resistance state (RESET).

3. Calculation principals

The CNTs in the cell adhere together mainly through van der Waals interaction in a disordered array of cross-link locations. This fibrous material behaves both elastically and plastically. The plastic, hysteretic part of the mechanics results from the creation and destruction of CNT-CNT van der Waals contacts as the material is compressed and stretched. The force which accomplishes this deformation is provided by the Coulomb interaction of non-equilibrium charge build-up in the CNT matrix due to the tunnel junction nature of transport. Thus we use an equation of continuum mechanics with experimentally determined elastic coefficients (Young's modulus and Poisson ratio) and with an external force from additional van der Waals couplings to describe the stress-strain relation on the fabric. We determine the charge accumulation by treating the current via a circuit model of series and parallel tunnel junctions, where each such junction is treated as a parallel (large) resistor and capacitor.

To make the description tractable (see figure 3) we make a quasi-one-dimensional approximation wherein the memory cell is divided into a set of horizontal, circular solid "slabs." Each slab has a variable number of tunnel connections to its adjacent slabs. Further, the strain in the cell is taken as only the component in the z-direction, u_z (i.e. electrode to electrode) and that component is taken to only depend on z. After calculating the force on a slab between an upper and a lower capacitor (both taken to have the same capacitance C for simplicity), the principal equation of the

Nantero, Confidential (2016)

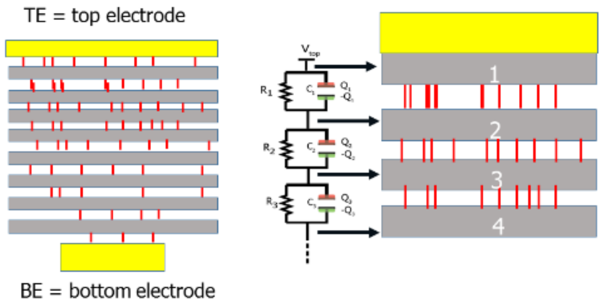

Figure 3 Schematic of cell simulation. Quasi-one-dimensional simulation with parallel tunnel junctions (red lines) giving composite tunnel junctions (right panel). The tunnel junctions are modeled, as usual, by a parallel capacitance and resistance ("leaky resistor").

simulation is thus:

$$\eta \frac{\partial^2 u_{z(z_n)}}{\partial z^2} = -\frac{CV^2}{d} \frac{\sum(r_{n+1}^2 - r_n^2)}{R_\Sigma^2} + F_{vdW} \qquad (1)$$

Where u_z is the z-displacement of slab n, $\eta = E(1-\sigma)/[(1+\sigma)(1-2\sigma)]$, with E Young's modulus and σ the Poisson ratio; and where V is the total voltage from top to bottom electrodes, C is the capacitance between slabs, separated by distance d, r_n is the resistance between slabs n and n+1, R_Σ is the total resistance and F_{vdW} is the van der Waals force on layer n.

The problem becomes self-consistent when we recognize that the resistance between layers is itself a function of the displacements of those layers. The description of the relationship between resistance and slab distance will be elucidated in the presentation.

4. Calculation inputs and results

We employ simulation and experiment to determine the parameters that are appropriate for the simulated device. For example, scanning force microscopy on the CNT material gives a Young's modulus which varies, according to CNT type, from about 4 to 24 giga-Pascals. Similarly, resistances as a function of distance and capacitances between layers are estimated from calculation and experiment to produce values that are faithful to the device structure.

The simulation proceeds by specifying the voltage, V, along with the device geometry (number of layers, Young's moduli of the layers, capacitances and maximum and minimum number of tunnel connections between layers, etc.) and the van der Waals force (which we will discuss in the presentation) and self consistently solving Equation (1) along with the relationship between the resistances and the level displacements. Resistance bottlenecks occur because the number of tunnel connections to the bottom electrode (BE) is constrained by the geometry and the relatively small

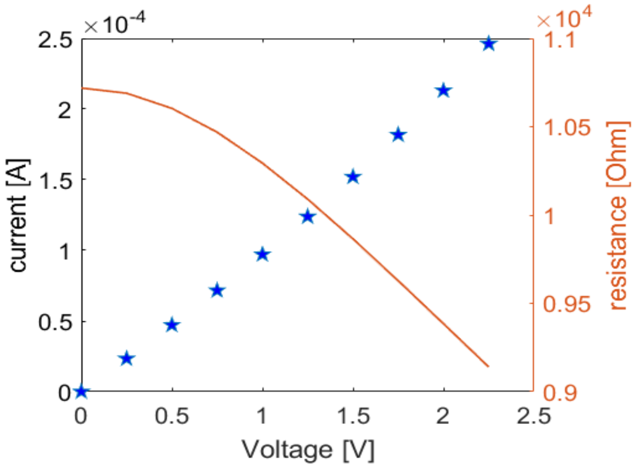

Figure 4 Current-Voltage and resistance-voltage (right scale) characteristic from slab model for CNT memory cell device. Resistance decreases as compressive force across bottom (switching) layer increases the number of tunnel connections and lowers resistance.

area of the electrode. This results in a compression of the CNT material close to the BE, which in turn produces an increase in the number of CNT-CNT connections in that layer (the switching layer). The net result of the CNT fabric stretch/compress behavior is an equalization of the resistivity throughout the cell.

The total resistance is simply the sum of the resistances between slabs and the current is the voltage divided by that resistance. An example of the calculation, without fitting parameters, is shown in figure 4. The current is on the left scale and the resistance on the right scale. This is the correct order of magnitude for the I-V behavior of the actual device in the SETmore situation.

5. Conclusion

In conclusion, we have developed a nanoelectromechanical model to describe the interaction of the Coulomb force on nonequilibrium charge carriers and the stretching and compressing of the CNT fabric of a NRAM memory cell. Extensions to the hysteretic (van der Waals) and dynamic (RESET) case will also be discussed.

References

[1] S. Ning, IEEE Transactions on Electron Devices, **62**, 2837 (2015).

[2] K. Takeuchi, "Demonstration of a High Speed, Low Power and Highly Reliable NRAM: Carbon Nanotube Based Nonvolatile Semiconductor Memory Device," 2014 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), Hsinchu, Taiwan.

[3] M. Stopa and T. Rueckes, Jpn. J. Appl. Phys. **55**, 04EE03 (2016).