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Differential Contact RRAM Pair for Advanced CMOS Logic NVM applications

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ABSTRACT

Stability has been one of the critical challenges in the implementation of large resistive random access memory (RRAM) arrays. Read window degradation in cell repeatedly cycled can significantly limit the design margins and application of such memory technologies. In this study, the new differential CRRAM cell composed of two CRRAM storage nodes in pair is proposed to enlarge read window and enhance reliability. Through differential read operations, the cell is less susceptible to read error caused by process variations as well as environmental changes. The new cell with differential storage pair also exhibits extended data retention and cycling capability and is found be an easily compatible logic NVM solutions for future CMOS technologies.

Introduction

With the growth of portable electronic products, logic nonvolatile memory (NVM) becomes in high demand [1-3]. RRAM has been regarded as a highly competitive candidate as a result of its compatibility to CMOS technologies in advanced nodes [4]. Previous proposed embedded RRAM technologies feature fast program speed, low power consumption and compact cell size [5-6]. However, its reliability and variability problems are the main challenges in the development for sizable RRAM arrays. In traditional 1T1R CRRAM, read window degeneration in cycled cells and random variability found in scaled cells are key obstacles [7]. Hence, redesign and modification of cell and array structure are needed for CRRAM technologies in advanced CMOS nodes. In this work, a differential contact resistive random access memory pair has been proposed and demonstrated by a standard 28nm high-k metal-gate logic process. Adapting a differential storage pair, the cells exhibit reduced read current sensitivities toward process and/or cycling variations in CRRAM cells, increased sensing window, and enhanced data retention.

Cell Structure and Operation Principle

In this study, an 8x8 array with differential CRRAM pair is implemented by pure 28nm CMOS logic process. The RRAM node is serially connected to a select transistor for controlling the forming, set and reset current during resistive switching operations. The differential pair is formed by placing two identical contact RRAM storage node isolated by a STI, as illustrated in Figure 1(a). The TEM picture of Contact RRAM storage pair realized by 28nm high-k metal gate process is shown in Figure 1(b). Furthermore, differential CRRAM pair can be arranged in an array with complementary readouts. Its corresponding layout and array schematic are shown in Figure 2(a) and Figure 2(b), respectively. In this memory array, two CRRAM storage node share a common SL connected by metal 1 layer and form a storage node pair (SN_l and SN_r) which enables data readout by complementary bit-lines (BL, BLB). To investigate the initial mismatches between the left, SN_l, and the right, SN_r, storage nodes, the read current distributions compared in Figure 3, reveal similar read current ranges both in the left and right nodes. A differential CRRAM pair has four states, as illustrated in Figure 4(a). The operation flow chart of resistive switching between the initial, erase, zero and one states are shown in Figure 4(b).

Based on the RRAM vacancy model [8-9] proposed over the years, the low resistance path, conductive filaments (CF), is formed by applying a large enough electric field across the resistive film, inducing the generation of oxygen vacancies. Reversely, a large enough reset current passing low-resistance path across the resistive film can disrupt the CF by the recombination of oxygen vacancies. Initialization of the array starts with a blanket forming step to put all SN into LRS, followed by a reset operation of both SN_l and SN_r in all cells. For writing zero to a different cell, only SN_l is set to LRS, whiling for writing one to a cell, only SN_r is set to LRS. Hence, the SN pair are in a complementary state. Operation conditions for the writing complimentary data into the CRRAM storage pair in this differential cells is illustrated in Table 1. Data shows that the set/reset time for SN_l and SN_r in an array are very close to each other, as shown in Figure 5. Data in Figure 6 reveals that the read current window can be enhanced 2.5X in a sizable array. Furthermore, cycling capability also effectively enhanced as shown in Figure 7. Comparing with the single end cells, read window degradation in cycled cells can be ameliorated by adapting a complementary cell.

Reliability Characteristics

Differential current of the CRRAM pairs remains stable after 10^4 times of over-reset/set stress as shown in Figure 8. Read current stability is tested under constant read disturb as shown in Figure 9. No observable change in the differential current of the complementary cells. Retention characteristics under elevated temperature bake tests for 200 hours reveal that differential cells exhibit superior data integrity as shown in Figure 10. To ensure the stable sensing current window during cycling, incremental step pulse programming (ISPP) method is applied for both set and blanket reset with 10μs and 100μs, respectively. Finally, the complementary cells can endure over 100k set/reset cycles with minimal change in its states by the ISPP operations, as shown in Figure 11.

Conclusions

The differential CRRAM pair**,** fully compatible to standard 28nm high-k metal gate CMOS logic process, is proposed and demonstrated. Differential CRRAM pair solves the reliability problems of traditional 1T1R cells. In addition, differential CRRAM pair has superior reliability and endurance under ISPP and bake tests. Furthermore, differential CRRAM pair increases read window and simplicity of its symmetric structure, and it's suitable for logic NVM applications.

Acknowledgement

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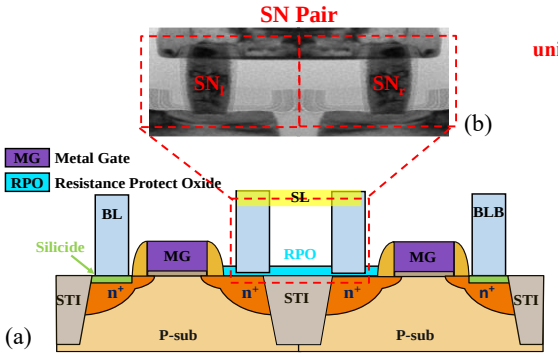


Figure 1 (a) Cross-sectional illustration of the differential Contact RRAM pair proposed in this study. (b) TEM picture of Contact RRAM storage pair realized by CMOS process.

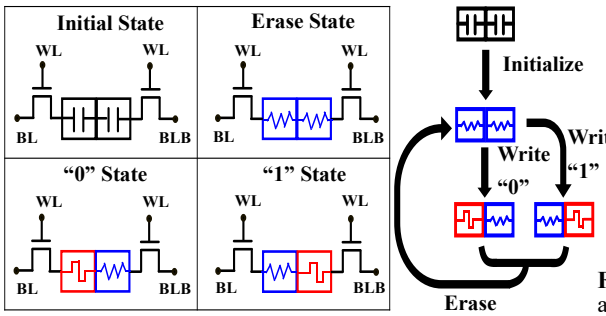


Figure 4 (a) Circuit illustrations of the 4 different states in the CRRAM differential pair. (b) Operational flow chart for writing and erasing the CRRAM storage pair.

Operation \ Terminal		BL	BLB	SL	WL
Initialize	Blanket forming	0V	0V	3.2V	0.8V
	Blanket reset	0V	0V	1.6V	1.8V
Write"0"		0V	Float	2.8V	0.8V
Write"1"		Float	0V	2.8V	0.8V
Erase		0V	0V	1.6V	1.8V
Blanket read		0.2V	0.2V	0V	1.2V

Table 1 Operation conditions for writing complementary data into the differential CRRAM storage pairs.

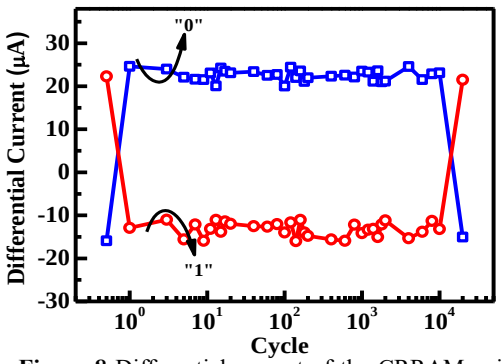


Figure 8 Differential current of the CRRAM pairs remains stable after 10^4 times of over-reset/set stress.

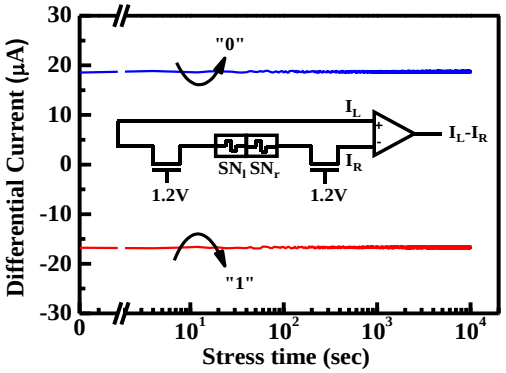
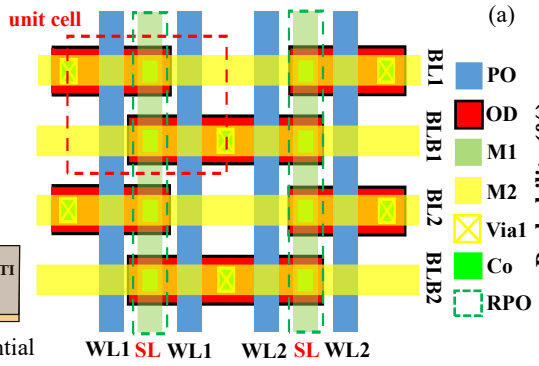


Figure 9 Read current stability is tested under constant read disturb. No observable change in the differential current of the complementary cells.



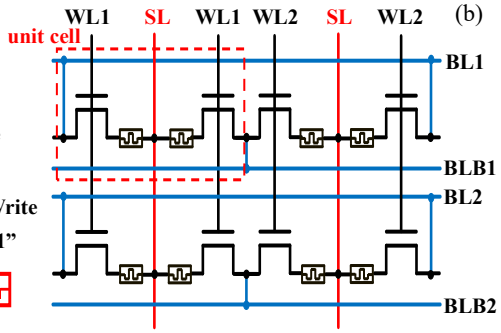


Figure 2 (a) Layout (b) and circuit schematic of a 2 x 2 NOR array with CRRAM storage node pair (SN$_l$ and SN$_r$ on the left and right respectively), allowing differential readout by complementary bit-lines (BL, BLB).

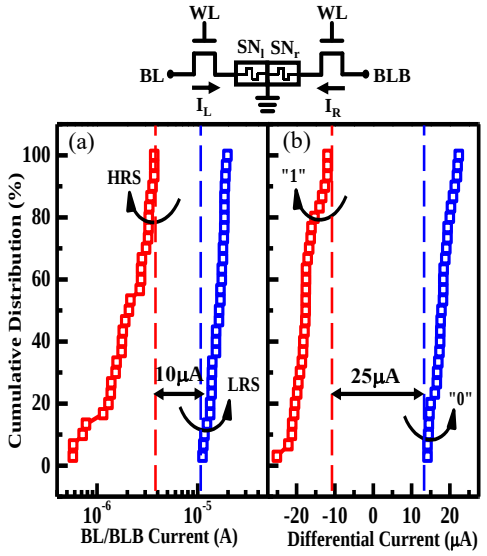


Figure 6 Read current distributions of (a) 1T1R CRRAM cells and that of (b) differential CRRAM pairs. Measured data reveals that the read current window can be enhanced 2.5X in a sizable array.

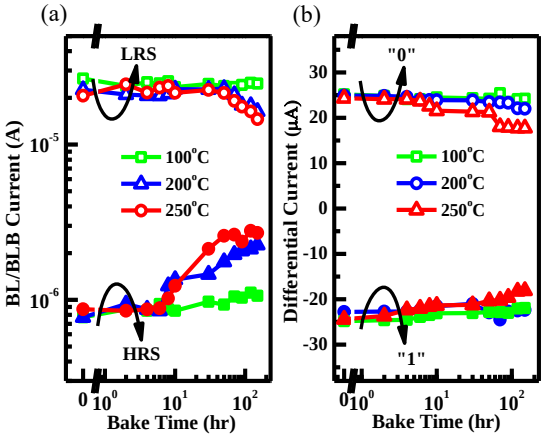


Figure 10 Data retention of (a) 1T1R cells, and that of (b) differential pairs. The complementary cells are found exhibit superior data integrity under bake tests.

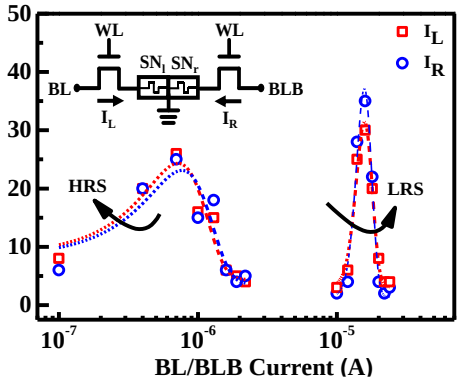


Figure 3 Read current distributions of the left, SN$_l$, and the right, SN$_r$, storage nodes in the CRRAM pairs in the proposed differential array.

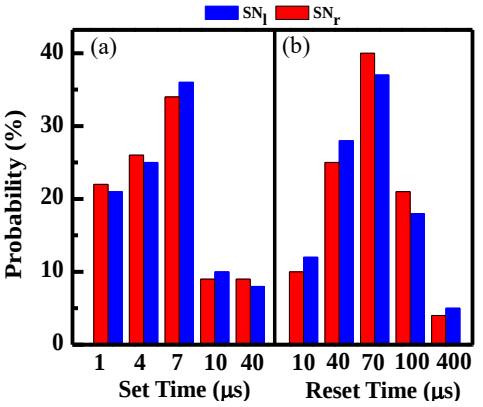


Figure 5 Comparison of set and reset time of the left, SN$_l$, and right, SN$_r$, storage nodes. Data shows matching distributions.

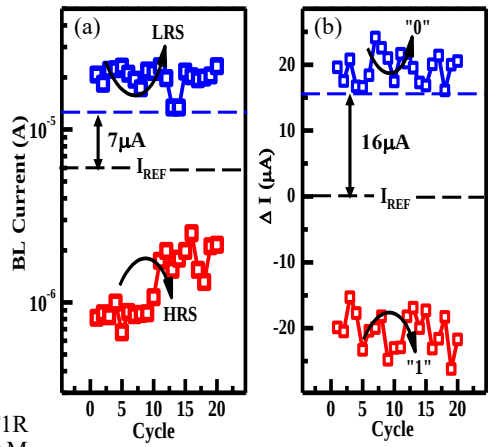


Figure 7 DC cycling results of (a) 1T1R cells and that of (b) differential pairs. Read window in complementary cells is 2X larger.

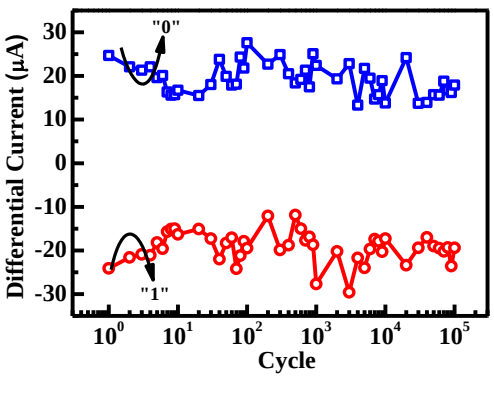


Figure 11 Differential cells can endure over 100k set/reset cycles with minimal change in its states by the ISPP operations.