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Twin-bit Via RRAM in 16nm FinFET Logic Technologies

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Abstract

A fully-compatible Via RRAM cell in 16nm CMOS FinFET logic process has been successfully demonstrated for a high-density and low-cost logic nonvolatile memory (NVM) applications. In this new cell, the transition metal layers are form at both sides of a Via, given two storage bits for one via. In addition to its compact cell area (14nmx32nm), the twin-bit Via RRAM cell features low voltage operation, large read window, excellent data retention and cycling capability. As a promising embedded NVM solution, the twin-bit Via RRAM cell is highly scalable with fine alignment and nano-scale feature length become possible in advanced CMOS technologies.

Introduction

With low-power, high-compatibility and high programming speed, RRAMs are regarded as one of the possible solutions for logic NVM applications under intense investigations. Many different structure of RRAMs with low operation voltage, compact cell size and fast writing speed are reported in many studies [1-2]. Most of these cells are demonstrated in planar CMOS logic processes [3-4] or by incorporating transition metal oxide (TMO) layer in backend of the line processes [5]. With CMOS technology node advancing, the planar logic process has been replaced by 3D FinFET process for enhanced gate control, leading to new challenges for the development of logic NVMs. Novel structures for 3D FinFET process is needed to develop fully-compatible NVM cells. In the study, the twin-bit RRAM with high density, low power and high transition speed is successful implemented in pure 16nm FinFET CMOS logic process. With TMO layers on both sides of a Via, served as the twin resistive switching nodes, a novel RRAM cell has been proposed and demonstrated in this structure.

Cell Structure and Operation Principle

The proposed twin-bit Via RRAM cell is fabricated by standard FinFET CMOS logic process. The structure of Via RRAM is illustrated in figure 1(a). As shown in the picture, the cell consist of two storage nodes both side of Via1. The other electrode, M1, is then connected to an n-channel FinFET which control the set/reset and read of the selected operation. The TMO layer is consisted of TaON and SiO_2 at the sidewall of Vias, sandwiched between Via and Metal electrodes. By placing a single via between closely placed metal 1, the twin-bit RRAM cells are easily formed. Based on previous studies on resistive switching mechanisms in oxygen vacancy based RRAMs [6-7], the low resistance path is formed by applying a large enough electric field across TMO layer, which established a conductive filaments (CF). Reversely, with large reset current through the low resistance path, the existing CF will then be partially broken apart by the recombination of oxygen vacancies.

The twin-bit Via RRAM cell is placed in a 2x2 array with two RRAM sharing a single Via between the right and left bit, as illustrated in Figure 1(b). A 2x2 array layout of the twin-bit RRAM in Figure 1(c) showing how the two cells sharing one via connection to SL.

Via RRAM Characteristics

The DC set / reset characteristics of the twin-bit via RRAM cells are compared in figure 2. Data demonstrate that the set voltage is lower than 2.5V and the reset operation can be achieved under 0.8mA. In order to obtain the viable RRAM cell, samples with different spacing between Via1 and Metal1 are first screened by the initial read current measured on multiple samples, as summarized in Figure 3. The results suggest that sample with a drawn spacing of 14nm can best to avoid irrecoverable direct short on both the right and left bits. Figure 4 shows the I-V characteristics under forward and reverse read and slight rectifying effect at the metal/TMO interface is found. As demonstrated in Figure 5, stable read current levels of on cells in both LRS and HRS by DC sweeps is readily established. Set/rest and read conditions of Via RRAM are then summarized in Table 1.

Higher SL voltage affects the set / reset speed by providing the higher electric field and larger reset current, which results in an faster operation speed of 10ns and 0.1μsec, as shown in Figure 6. Figure 7 shows the read disturb test results, revealing there is no obvious read shift under constant read. The overset / reset stress tested for over 10^4 pulses with no significant current shift are demonstrated in Figure 8. Figure 9 shows the stable LRS and HRS under high-temperature baked test at 100℃ for over 100 hours. To ensure the cell providing stable read current levels during data cycling, Incremental Step Pulse Programming (ISPP) algorithm is applied for both set and reset operations with pulse width of 10μs and 0.5μs, respectively. By setting the incremental SL voltage step of 50mV, its read window maintains more than 10^3X after 10^6 ISPP cycles, as demonstrated in Figure 10.

Conclusions

A novel structure of RRAM cell, fully compatible to CMOS logic process, is proposed and demonstrated in 16nm FinFET CMOS logic process. By the TaON and SiO_2 layer at both sidewalls of a single Via, the twin-bit RRAM cells is readily implemented. In addition to superior reliability and endurance levels, the twin-bit Via RRAM cell are proven to be a promising candidate for high density NVM for advanced FinFET logic circuits.

References

[1] K. P. Chang, et al, SSDM, pp.1168-1169, 2008
[2] L. Y. Yang, et al. EDL, Vol.33, No.2, pp.245-247, 2011
[3] C. J. Lin, et al. IEDM, pp.1-4, 2009
[4] M. Chen, et al. EDL, Vol.29, No.5, pp.522-524, 2008
[5] Z. Fang., et al. EDL, Vol. 32, No.4, pp.566-568, 2011
[6] I. S. Park, et al. JJAP, Vol. 46, pp.2172-2174, 2007
[7] S. G. Park, et al. NVMTS, pp.1-5, 200

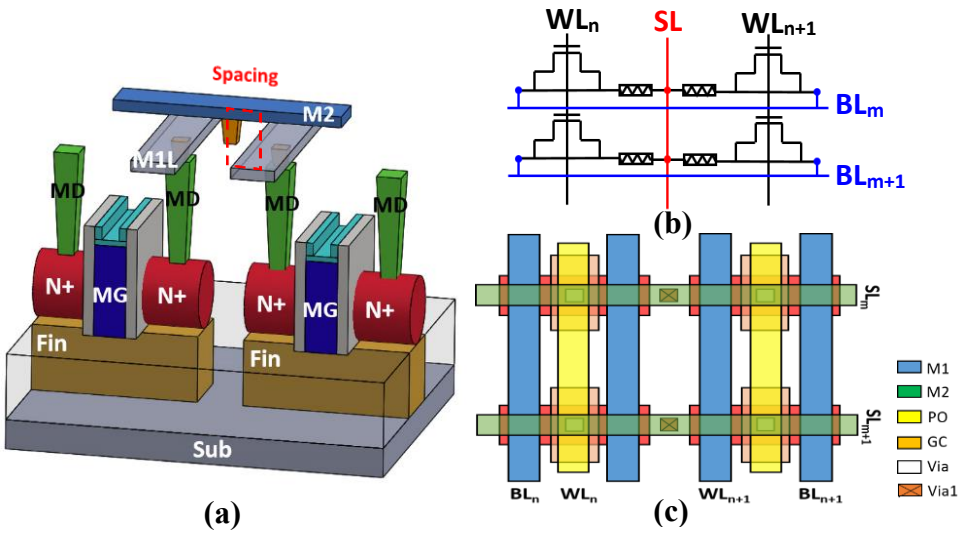

Figure 1 (a) A 3D illustration of 1T1R Via RRAM cells implemented by the standard FinFET CMOS process. (b) The circuit schematic of a 2×2 NOR type array with two RRAMs sharing the same SL Via between the left and right cells. (c) 2D layout for the 2×2 array with highly compact cells in advanced FinFET technologies.

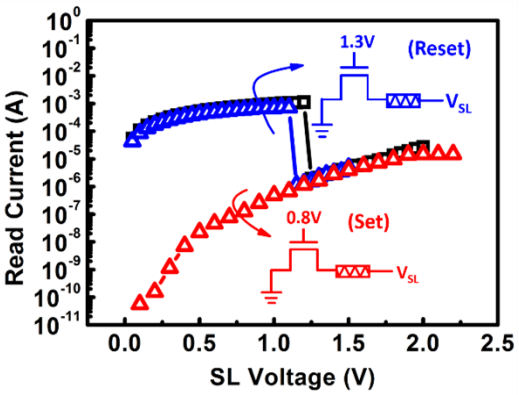

Figure 2 IV characteristics of the Via RRAM cell under unipolar DC sweep tests, revealing set/reset operations can be complete under 2.5V.

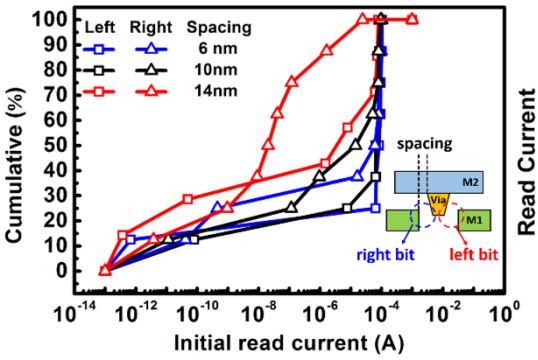

Figure 3 Comparison of initial read current distributions of the left / right bits on samples with different lateral spacing, S= 8,10 and 14nm, between Via2 and Metal 1 mask layers.

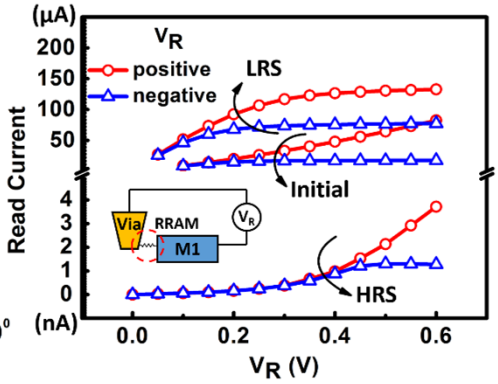

Figure 4 IV curves of a Via RRAM under forward / reverse sweeps. Slight rectifying effect at the metal/TMO interface is found during reading.

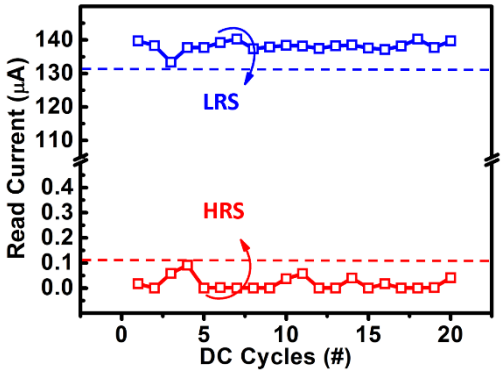

Figure 5 DC cycling results of Via RRAM reveal stable read window under a low-voltage read conditions at WL and SL both equals 0.6V.

		WL	BL	SL
Set	Sel.	0.8V	0V	2V
	Unsel.	0V	Floating	2V
Reset	Sel.	1.3V	0V	1.2V
	Unsel.	0V	Floating	1.2V
Read	Sel.	0.6V	0V	0.6V
	Unsel.	0V	Floating	0.6V

Table 1 Summarize listing of the operation condition summary for the twin-bit Via RRAMs in a NOR arrays.

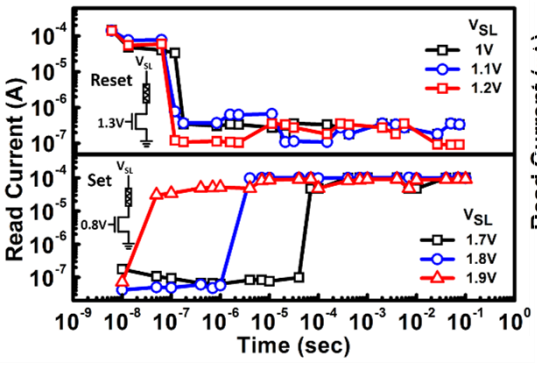

Figure 6 Time to reset / set characteristics, suggesting that resistance switching between high/low states can be achieved within few micro seconds.

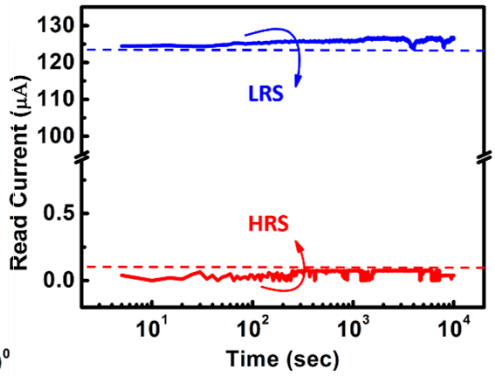

Figure 7 Read current stability is tested under constant read disturb. No observable change in the read current in the RRAM cells.

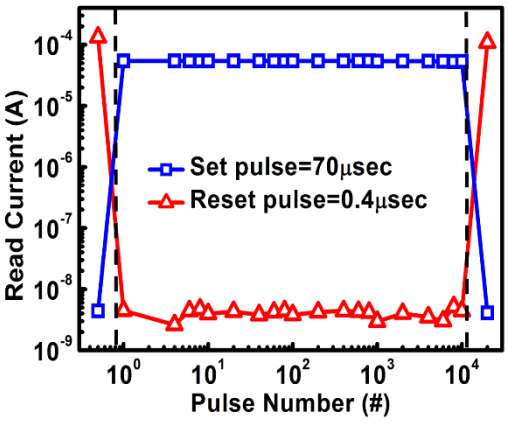

Figure 8 Over set /reset disturb is tested for over 10^6 cycles showing stable resistance states.

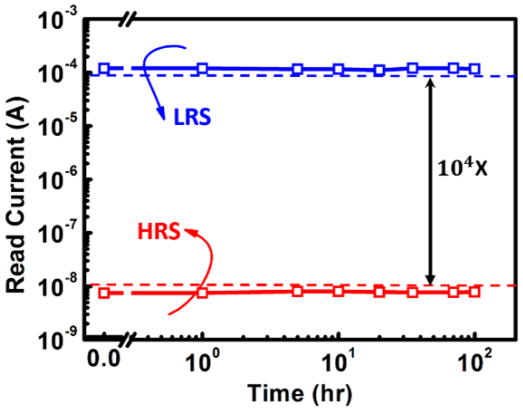

Figure 9 Data retention capability of twin-bit Via RRAM are tested at 100℃ bake for over 100 hours with no obvious shift observed.

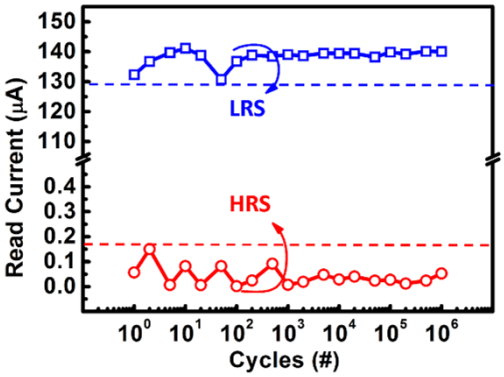

Figure 10 Cell endurance is tested for more than 10^6 set/reset cycles. Stable read window of more than 10^3X is maintained by optimized ISPP scheme.