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OxRAM integration above FDSOI transistor drain: Integration approach and process impact on electrical characteristics

M. Barlas[1*], L. Grenouillet[1], E. Vianello[1], V. Delaye[1], T. Dewolf[1], G. Audoit[1], N. Rambal[1], S. Bernasconi[1], C. Vizioz[1], N. Posseme[1], C. Arvet[2], S. Barnola[1], B. Bouix[1], O. Pollet[1], C. Comboroure[2], N. Allouti[1], P. Rodriguez[1], V. Beugin[1], V. Loup[1], C. Tallaron[2], S. Chevalliez[1], R. Coquand[1], C. Jahan[1], S. Reboh[1], A. Toffoli[1], S. Barraud[1], L. Brevard[1], Y. Morand[1], M. Vinet[1], O. Faynot[1], and L. Perniola[1]

[1] CEA-Leti, Minatec Campus, 17 Rue de Martyrs, 38054 Grenoble, France [2]STMicroelectronics, Crolles, F-38920, France
*E-mail: marios.barlas@cea.fr

Abstract

In this work, we present for the first time HfO_2-based OxRAM co-integrated above the drain of FDSOI transistors at 300mm scale. Functional 1T-1R devices are demonstrated up to 10^8 cycles. The impact of process-induced structural defects in the electrical and statistical behavior of the devices is explained by means of simulation and TEM/EELS characterization, allowing to determine the requirements for more process-robust devices.

1. Introduction

HfO_2-based OxRAM are promising non-volatile memories with the capacity for integration both in the back-end and the front-end of HKMG CMOS technology owed to material compatibility [1, 2]. Integrating the memory element in the transistor vicinity can prove particularly beneficial for near memory computing architectures, not only as the best selector candidate to date is still the FET but also because it can enable high density, limit parasitic interconnect contributions and enable innovative, more flexible circuit design. In this context, we demonstrate a new OxRAM / FDSOI transistor co-integration scheme and link the crosstalk between process and material related structural characteristics to the statistical behavior of the cells.

2. Integration approach

The memory element is implemented right above the transistor drain in a 300 mm FDSOI route (Fig. 1), with 2 additional mask levels. For this first demonstration, the 1T-1R footprint is ~0.02 μm^2, with thin oxide FDSOI transistor gate length and active width at 60 nm and 380 nm, respectively. The OxRAM structure consists of a TiN (30 nm)/Ti /HfO_2 (5 nm, ALD deposited, amorphous)/TiN (10 nm) stack with Ti thickness splits of 5 nm and 10 nm. OxRAM radius ranges from 500 nm down to 60 nm. A SiO_2/SiN double-hard mask strategy is introduced for OxRAM stack patterning and serves a triple functionality: Firstly, it targets to minimize the impact of etching chemistry on the stack sidewalls by allowing oxygen-based dry stripping right after hard mask etching. Secondly, it enables simultaneous contact opening at 3 different levels: transistor source, transistor gate, and OxRAM top electrode (Fig. 1). Finally, it allows patterning of nitride spacers around the stack aiming to protect OxRAM sidewalls with no impact on the hard mask. An STEM image of the developed 1T-1R structure is shown in Fig. 2.

3. Electrical characterization and statistical analysis

The FDSOI transistors fabricated present good electrical behavior and very small threshold voltage dispersion (Fig. 3). Quasi-static and pulsed operation reaching up to 10^8 cycles of the memory cell is shown in Fig. 4a, and Fig. 4b for large structures. However, memory high resistive state (HRS) shows significant device-to-device variability (Fig. 4b, grey zone). Forming voltage increases when device area decreases in line with already published results [3], and when the Ti oxygen scavenger thickness decreases (Fig. 5). However, Weibull statistics on the forming voltages show an unexpected behavior: The Weibull *slope* which is expected to be constant with area [3, 4] decreases significantly with decreasing device area, with the trend becoming stronger for the thinner Ti stack (Fig. 6 a, b & Inset). This actively suggests a modification of the Ti/HfO_2 interface properties originating from the OxRAM sidewalls, as smaller devices are more strongly impacted. To get more insight on potential structural defects, TEM/EELS was performed for different OxRAM areas (Fig.7).

4. Impact of process-induced defects on Weibull Statistics

TEM & EELS analysis reveals area-dependent cracking/delamination in the vicinity of the top TiN layer (Fig. 7 a, b), suggesting the presence of significant plane stress. Contact zone modeling (CZM) [5, 6] can reproduce the defect behavior as a function of the TiN/Ti interface adhesion properties [6, 8] and projected stress level in TiN. Analysis suggests that high compressive stress in TiN can catalyze the propagation of sidewall defects originating from the dry etch or wet process steps prior to memory encapsulation. Loss of contact is assumed at the sharp, PVD-deposited Ti/TiN junction owed to its high mechanical mismatch (Fig.8) that is expected to have inferior adhesion properties as compared to the mixed Ti/HfO_2 interface [7]. Simulation shows that the derived crack propagation length is in-line with TEM observations (Fig. 7a, b & 9a-c) for TiN stress in the range of -6 GPa. This exposes the Ti layer to contaminants such as oxygen (Fig. 7 c, d), impacting the Ti/HfO_2 interface and therefore OxRAM electrical characteristics. Finally, the dependence of Weibull parameters to device area and Ti thickness can be attributed to a diffusion-limited segregation of oxygen towards the Ti/HfO_2 interface limited by the crack extent and Ti layer thickness as well as a modification of the effective electrical surface of the cell.

5. Conclusions

In this work, we present a new OxRAM integration, in the early MOL of a 300 mm FDSOI route. By Weibull analysis of the forming events, TEM/EELS analysis and simulation, we correlate the impact of structural defects originating from process steps and catalyzed by the pre-stressed TiN electrodes, to the quality of the Ti/HfO_2 interface. Maintaining a trap-rich interface with strong adhesion as well as managing the structure stress level is critical for process-robust aggressively-scaled OxRAM with good electrical characteristics.

References

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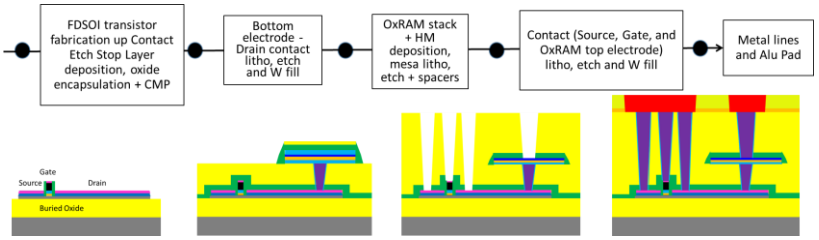

Fig.1: Integration flow. From left to right process blocks post transistor silicidation

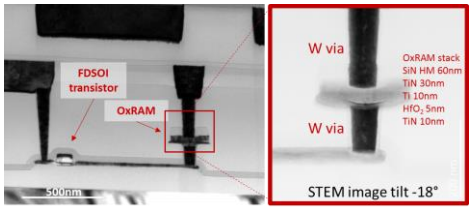

Fig.2: STEM view of a 1T-1R Structure

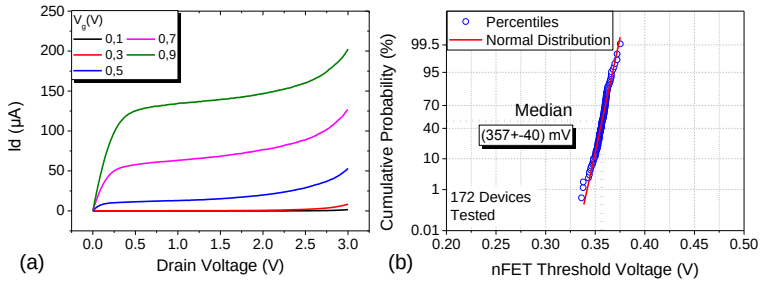

Fig.3: (a) I_d-V_d current transfer characteristics of the FET (b) nFET Threshold voltage statistics. Good current delivery and very small V_{th} dispersion.

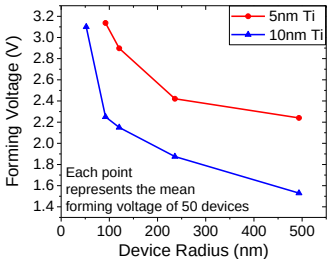

Fig.5: Evolution of forming voltage mean values with nominal device radius and thickness of the Ti layer.

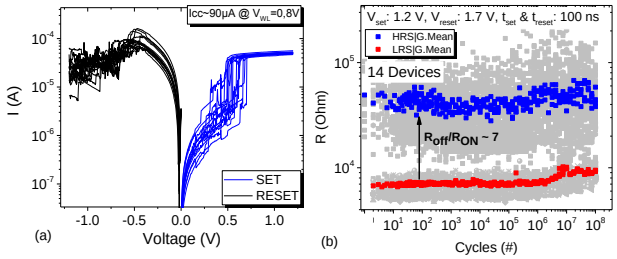

Fig.4: Switching Characteristics of a 500 nm radius OxRAM device (a) Quasi-static (b) Pulsed Operation.

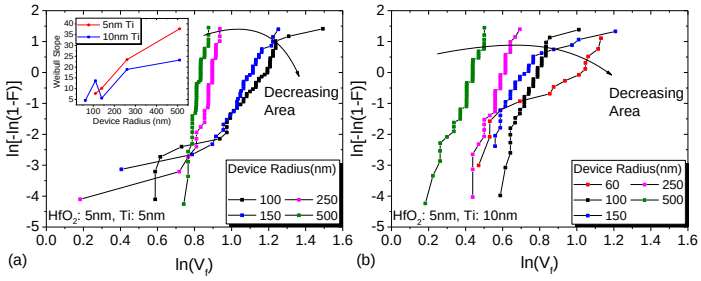

Fig.6: Weibull plots with device size and Ti thickness for 5 nm (a) and 10 nm (b) Ti scavenging layer. (Inset) Evolution of slope of (a), (b).

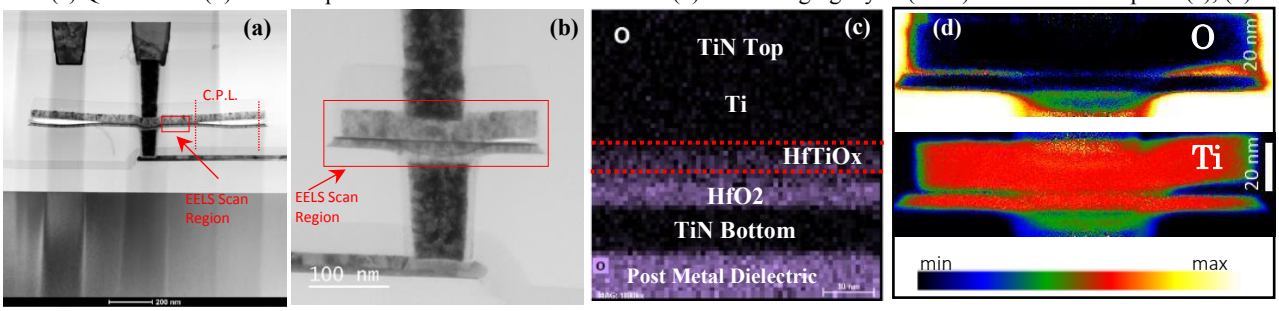

Fig. 7: STEM Image of (a) 500 nm and (b) 100 nm radius device in the TiN(30 nm)/Ti(10 nm)/HfO_2 (5 nm)/ TiN(10 nm) stack. (c), (d) EELS analysis corresponding to (a), (b). TiN/Ti interface is clean in (a) while (b) shows traces of O contamination in the crack region.

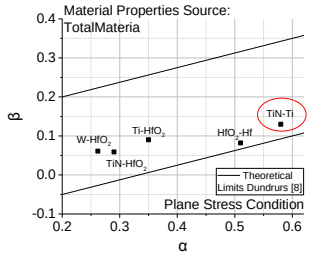

Fig.8: Comparison of ideal sharp interface mechanical mismatch parameters [8].Ti/TiN shows the highest mismatch.

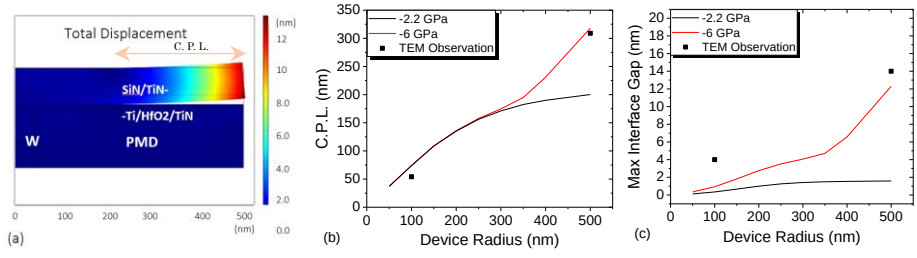

Fig.9: COMSOL simulation: Cracking/delamination of (a) 500 nm radius device (b) Crack propagation length evolution with device size. Defined where the interface contact pressure is zero for the first time. (c)TiN layer delamination post TiN/Ti interface separation. Crack propagation length (C.P.L.) is controlled by interface adhesion while Gap from bulk material properties.

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