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FinFET Split-Gate MONOS for Embedded Flash in 16/14nm-node and Beyond

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Abstract

FinFET split-gate metal-oxide nitride oxide silicon (SG-MONOS) for embedded Flash have been fabricated. Excellent subthreshold swing and small threshold-voltage variability are confirmed. It is demonstrated that an electric field enhancement at Fin top-corner is well suppressed by incremental step pulse programming. Data retention characteristics at 150 ºC after 250 K program/erase cycles shows sufficient reliability for advanced automotive system.

1. Introduction

Progress of leading edge automotive systems for such as autonomous driving requires performance enhancement of embedded Flash memory (eFlash) maintaining its high reliability. Metal oxide nitride oxide silicon (MONOS) is a charge-trapping type Flash and MONOS with split gate structure (SG-MONOS) has a long track record as highly reliable eFlash for automotive [1, 2, 3]. In the state-of-the-art logic CMOS, Fin structure is employed to realize high performance [4, 5], but SG- MONOS having Fin structure has not been reported until recently [6]. In this paper, FinFET SG-MONOS Flash has been demonstrated. First, fabrication process of the device and its key electric characteristics are presented. Then, fin top-corner effect is discussed by 3D TCAD simulation and measurement. Finally, the reliability of FinFET SG-MONOS is presented.

2. Device Fabrication

Schematic view and fabrication process flow of FinFET SG-MONOS Flash are shown in Figs. 1 and 2. Fin structures are first formed on bulk silicon substrates by patterning active area and recessing STI oxide. Control gate (CG) used as word line (WL), oxide-nitride-oxide (ONO) layer and the memory gate (MG), and spacer are formed with almost same sequence as that for conventional planar SG-MONOS. Bird's-eye and MG cross-section views of a fabricated device are shown in Fig. 3.

3. Results and Discussion

Figs. 4 and 5 shows the I-V characteristics of CG-MOS and MG-MOS for a FinFET SG-MONOS with W_{Fin} = 20 nm and a conventional planar SG-MONOS with W_g = 0.1 μm. The CG and MG of FinFET SG-MONOS have same gate lengths as the planer one. Owing to Fin structure, the FinFET SG-MONOS shows steeper subthreshold-swings than the planar device. The program and erase (P/E) speed of FinFET SG-MONOS is faster than planar in early P/E stages (Fig. 6). This is owing to enhanced electric field (EF) at the Fin-corner as will explain later. MG threshold voltage distributions at P/E states for the two structures are shown in Fig. 7. FinFET structure drastically reduce the threshold voltage variability due to its fully depleted characteristic compared to the planar SG-MONOS.

Fig. 8 shows 3D TCAD simulation of electric field in FinFET SG-MONOS at programing operation. At 1ns, EF in bottom oxide film at Fin top-corner is locally enhanced by a geometry effect. Such a local electric stress may adversely affect the reliability of the device. To suppress this Fin top-corner effect, incremental step pulse programing (ISPP) is investigated for FinFET SG-MONOS by simulation. Fig. 9 compares the time sequences of voltages applied to MG (V_{MG}) and source (V_S) of constant pulse programing and ISPP. In ISPP, V_{MG}, is gradually increased in three steps to the final positive high voltage (PHV) of the constant pulse. Fig. 10 shows the simulated EF within the device using constant pulse and ISPP. As for the constant pulse, EF at the first time point (t1) is quite high due to the fin corner effect. The field and corner effect gradually decrease with time due to trapped electrons. As for the ISPP technique, on the other hand, EF is kept at a low level and the Fin corner effect is well suppressed. A benefit of ISPP for P/E endurance characteristics is clarified in measurement. Fig. 11 shows degraded P/E time after 10K P/E cycles using constant pulse and ISPP in the fabricated FinFET SG-MONOS. In ISPP, lower erase time degradation after 10 K P/E cycles is experimentally confirmed with negligible loss of program speed compared with the constant pulse technique. One of the possible reasons for this is suppression of oxide deterioration due to weak and uniform electrical stress. Fig. 12 shows the results of P/E endurance tests carried out on the fabricated FinFET SG-MONOS with verifying Vth window of 4.5 V. No significant degradation of P/E time is observed over 250 K P/E cycles. The data retention characteristics after 250 K cycles at high temperature of 150 ºC are shown in Fig. 13. These data confirm that a V_{th} window of 2.0 V will be maintained for 10 years under the harsh conditions of automotive use.

4. Conclusions

FinFET SG-MONOS Flash for embedded Flash have been fabricated and operated. Excellent subthreshold swing and small threshold-voltage variability are confirmed. Electric

field enhancement at Fin top-corner is effectively suppressed by incremental step pulse programming. Excellent endurance characteristics over 250 K P/E cycles and highly reliable data retention at 150 ºC have been demonstrated. Based on these results, FinFET SG-MONOS has been confirmed to be a highly scalable and reliable embedded Flash for 14/16 nm node and beyond.

References

[1] T. Kono *et al.*, ISSCC, pp. 212-214, 2013.
[2] Y. Taito *et al.*, ISSCC, pp. 132-134, 2015.
[3] T. Yamauchi *et al.*, IEDM, pp. 703-706, 2016
[4] D. Hisamoto *et al.*, IEDM, pp. 833-836, 1989.
[5] C. Auth et al., VLSIT, pp. 131-132, 2012.
[6] S. Tsuda et al., IEDM, pp.280-283, 2016

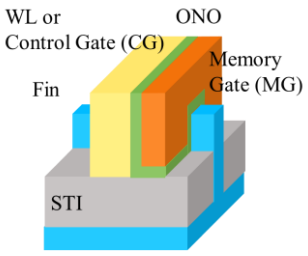

Fig. 1. Schematic view of FinFET SG-MONOS.

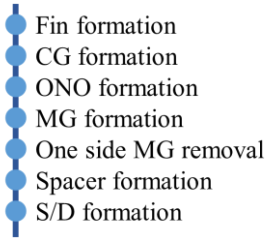

Fig. 2. Schematic process flow of FinFET SG-MONOS.

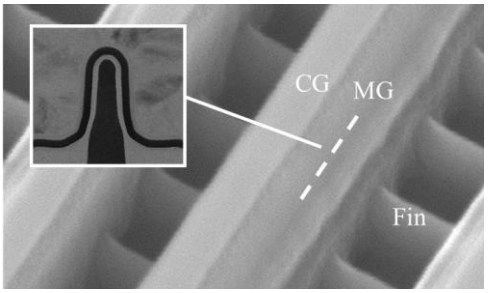

Fig. 3. Bird's-eye view of SEM image of FinFET SG-MONOS and Cross-sectional TEM image of MG-MOS.

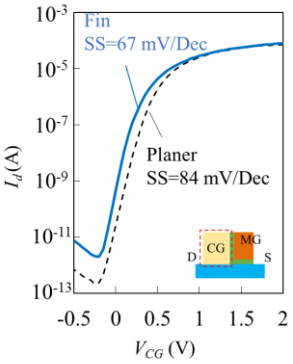

Fig. 4. I-V characteristics of CG-MOS.

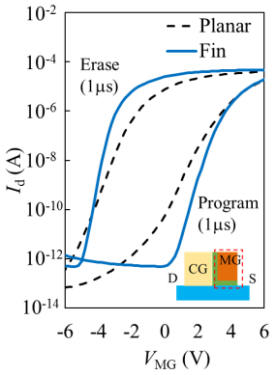

Fig. 5. I-V characteristics of MG-MOS at program and erase (P/E) states.

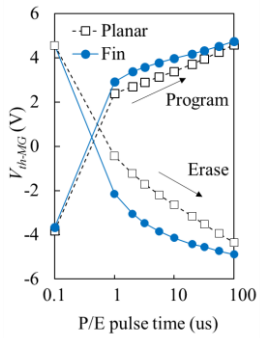

Fig. 6. P/E characteristics.

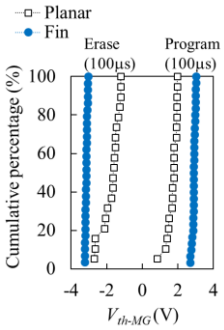

Fig. 7. $V_{th\text{-}MG}$ distribution at P/E states.

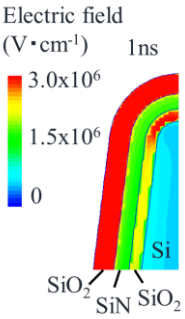

Fig. 8. Simulated electric field during program operation.

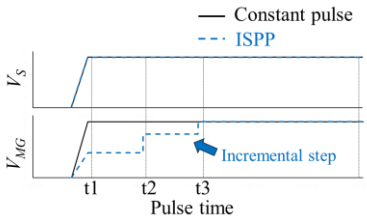

Fig. 9. Pulse diagram of constant pulse and incremental step pulse programing (ISPP).

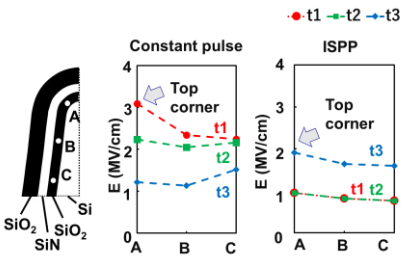

Fig. 10. Simulated electric field for constant pulse and ISPP.

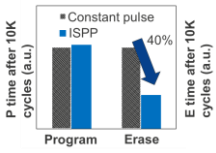

Fig. 11. P/E time with ISPP and constant pulse after 10K cycles.

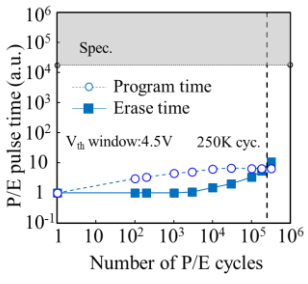

Fig. 12. Endurance characteristics of FinFET SG-MONOS.

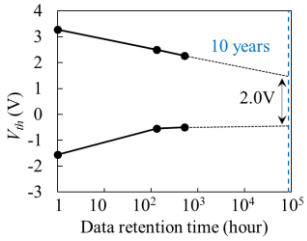

Fig. 13. Retention characteristics of FinFET SG-MONOS after 250K cycles at high temperature (150 ºC).