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P-channel Differential Multiple-TimeProgrammable Memory Cells by Laterally Coupled Floating Metal Gate FinFETs

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Abstract

A differential p-channel multiple-time programmable (MTP) memory cell is proposed and implemented in 16nm FinFET process. This new cell stores complementary data in floating gates coupled by slot contact structure enable different read current on a single cell. With a blanket boost scheme, charge retention problem in floating gate cells can be improved by periodic restoring lost charge when significant read window narrowing occurs. In addition to high programming efficiency, this p-channel MTP cells also exhibit good cycling endurance as well as disturb immunity.

Introduction

The demand for logic non-volatile memories (NVM) which are fully compatible to CMOS logic process, are growing fast in the IOT era [1]. In nano-scale CMOS logic processes, the gate dielectric layer is scaled to maintain good gate control for the transistors [2]. It becomes too thin to retain charge inside the floating gates for non-volatile data storage. The lost of charge storage capability greatly limits the applications of floating gate (FG) based NVM cells to less advanced technology nodes [3-5]. To resolve the problem of the poor data retention capability in FG cells, a differential FG multiple time programmable memory cell has been proposed and demonstrated by the 16nm CMOS FinFET technology. With a control line coupled to the high-aspect ratio metal gate, a highly area efficient coupling structure can be realized in FinFET technologies [6-7]. In addition, differential read out designed to complementary data storage in two floating gates in one cell increases the sensing window, immunity toward process variations. Finally, aperiodic blanket boosting scheme is proposed to restore data lost.

Cell Structure and Operation Principles

This differential MTP cell contains two identical floating gates transistors sharing a common select gate, which controls the selection of a cell during program and read operations. In high-k metal gate FinFET technologies, the floating gates are composed of high-aspect ratio metal gate control the channel of the transistor during read, see Figure 1(a). The laterally coupling structure illustrated in Figure 1(b) is formed by closely placing of long contact slots to the metal gate over STI regions, a large coupling capacitance between the floating gates and contact slots can be established. The p-channel MTP cell is programmed by channel-hot-hole induced hot electrons, which injects electrons to the floating gates, and turns the channel on by increasing the threshold voltage, as illustrated in Figure 2(a). Cells are erased by Fowler-Nordheim (FN) tunneling through the channel with a negative voltage applied on the control line (CL), see Figure 2(b). The differential MTP cells are arranged in an array with complementary bit-lines, as shown in Figure 3, as bit line (BL), and bit-line bar (BLB). Source and gate of the select transistors shared the same the source line (SL) and the word line (WL), respectively. When FG on BL is programmed, the cell is defined as in state "1", while electrons are in FG on BLB, the cell is in state "0", as shown in Figure 3. The optimal programming point can be found by monitoring the gate current of a dummy device as FG is swept, as shown in Figure 4. The measured gate current vs. control line voltage corresponds to the current injects into the FG. As expected, the injection current peaks at V_{FG} ~V_{th}~ -1V, corresponding to a V_{CL} of -2V. The I_DV_G characteristics in Figure 5(a) demonstrate that positive shift in V_{th} is successfully obtained. The read current distributions for cells in state"1" are compared in Figure 5(b). Time-to-program and time-to-erase characteristics are compared in Figure 6. The programming speed at V_{CL}= -2V can be as short as 1msec.For erase operations, V_{CL} set a high negative voltage to -14V for an erase time of less than 500ms.For read operations, V_{WL}=-1.8V, V_{CL}=V_{BL} =-0.8V for reaching a read current of 10μA. The operation conditions for this p-channel MTP cell are listed in Table 1.

Reliability Evaluations

For endurance testing, the read current after programming of both state are monitored during program/erase cycling. The test results are shown in Figure 7 revels that the sensing window remains stable after 100k P/E cycles. To examine the data retention capability of cells in an array, the change of read current distributions during 85C bake is summarized in Figure 8. Distribution of the single end read current reveals that the read window closes up very quickly. Threshold voltages change with time arranged in Figure 9 suggests that ΔI still remain positive for even for tail bits. However, small current differential on BL and BLB may still lead to read error as well as slow accessing rate. To encounter this problem, a data restoration scheme with propose. The blanket boost scheme to restore lost charge selectively to the programmed FG at V_{WL}= -1.8V, V_{CL}=V_{SL}= 0. The boosting pulses are applied to both BL and BLB of 400μsec, -3V. The charge restoration results in Figure 10 reveals the read current of the programmed side is boosted, while that of the erased side of the cell is not disturbed by this blanket operation. The periodic boosting is performed for cells bake at 85℃, as shown in Figure 11. As suggested by the data, a boosting of once every 48 hours is needed to maintain non-volatile data.

Conclusions

A p-channel differential MTP cell is presented with area efficient laterally coupling structures and extended sensing window. The charge restoration scheme is proposed to overcome the charge lost problem of floating gate based logic NVM cells for FinFET technologies.

Reference

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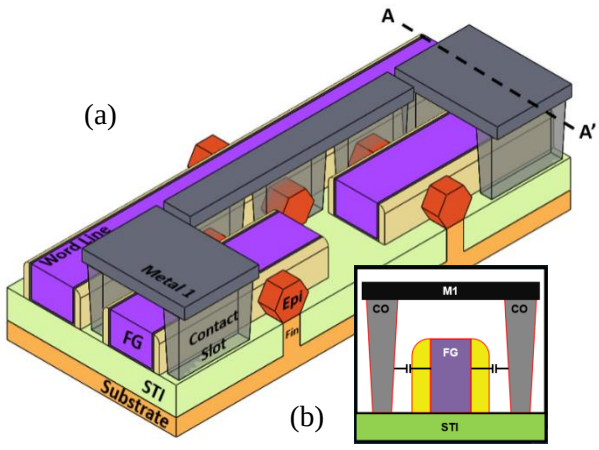

Figure 1 (a) 3D Illustration of a 3T p-channel differential cell with (b) high-aspect ratio metal floating gates coupled by closely placed contact slots.

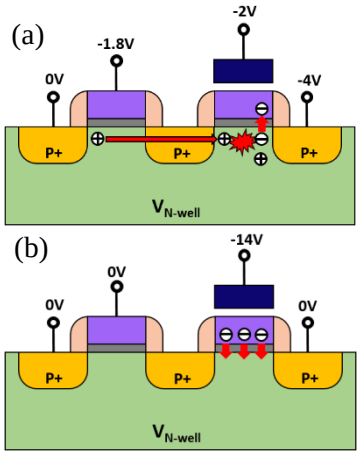

Figure 2 The Illustrations of (a) the programming and (b) erasing operations in the p-channel cell.

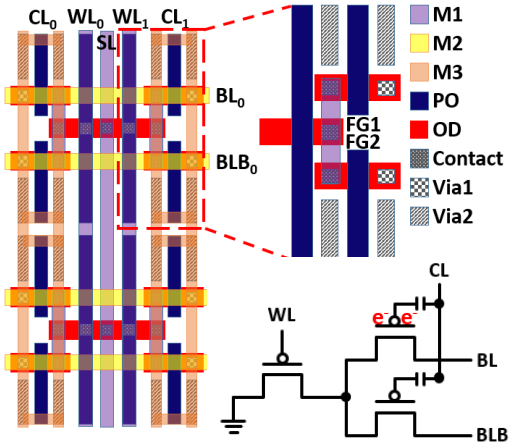

Figure 3 A 2x2 array layout that of an unit cell with also the circuit schematic of a cell in "1" states.

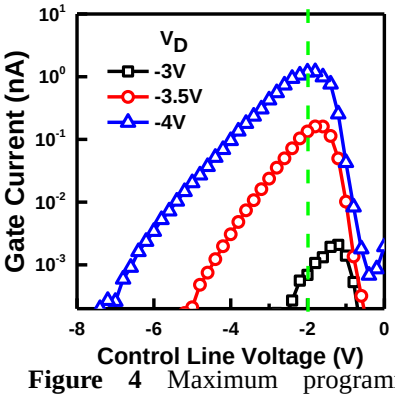

Figure 4 Maximum programming current occurs at V_{FG} close to threshold, corresponding to V_{CL} at -2V.

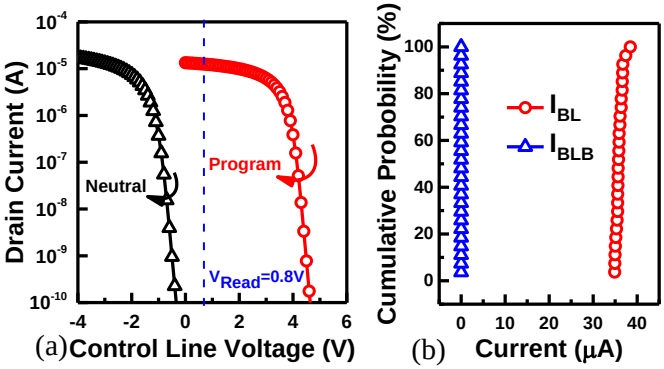

Figure 5 (a) Differential MTP can be successfully programmed by CHEIHH with positive V_{th} shift. (b) Read current distribution of the differential cell.

	WL		BL	CL
	Sel.	Unsel.	BLB	
Prog.	-1.8V	0V	-4V	-2V
Read	-1.8V	0V	-0.8V	0.8V
Erase	0V		0	-14V
Boost	-1.8V		-3V	0V

Table 1 Summary of operation conditions for complementary programming of single FG selectively to enable differential data read. FN erase with high negative voltage on control lines.

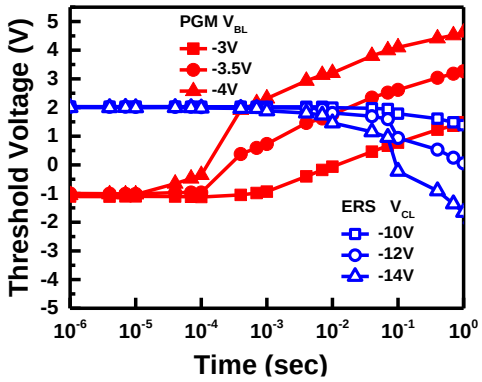

Figure 6 Time to program and time to erase characteristics at various V_{BL} during program and different V_{CL} for erase.

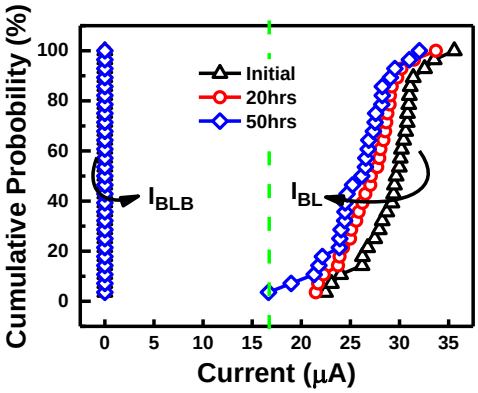

Figure 8 Read current distribution of the differential cell at its initial states and after 20 and 50 hours of 85℃ high temperature bake.

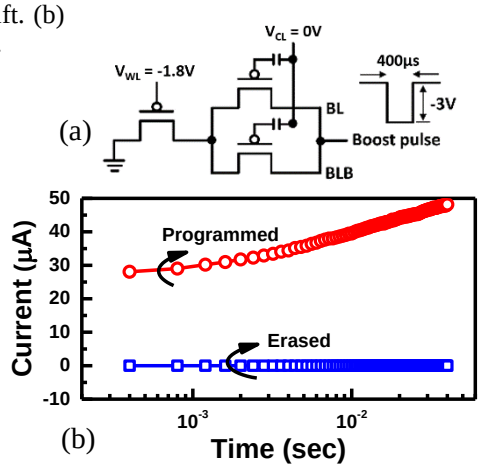

Figure 10 (a) The blanket boost scheme which (b) restores lost charge selectively to the programmed FG.

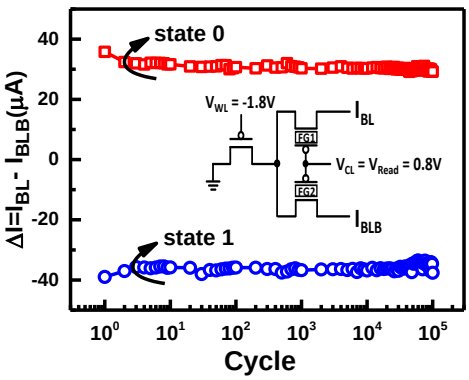

Figure 7 Endurance characteristics up to 10^5 cycles show stable read current window for differential cells at both states.

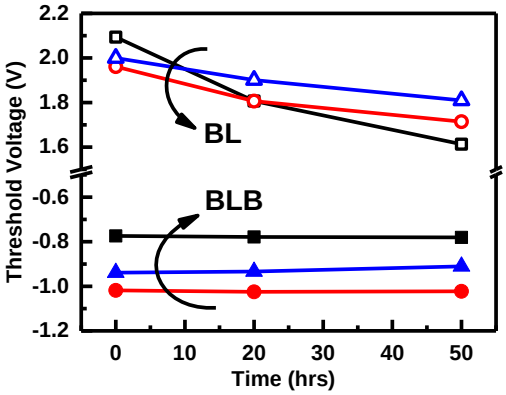

Figure 9 Threshold voltages of 3 tail bits are monitored at 85C. Differential current remains positive after 50 hours.

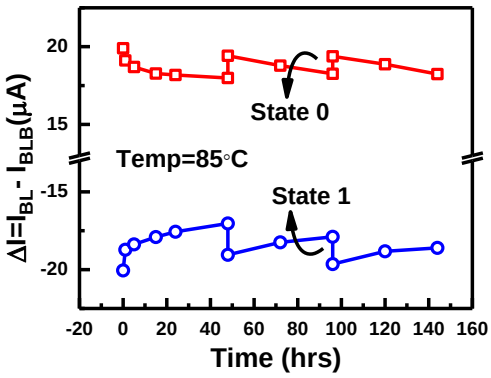

Figure 11 At 85℃, this p-channel MTP cell required blanket boosting every 48 hours to avoid data lost.