Extended Abstracts of the 2017 International Conference on Solid State Devices and Materials, Sendai, 2017, pp181-182

D-2-03

In-situ formation of Hf-based MONOS structure for nonvolatile memory application

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Abstract

This paper investigated the electrical characteristics of in-situ formed Hf-based Metal-Oxide-Nitride-Oxide-Silicon MONOS nonvolatile memory (NVM) for the first time. Memory window (MW) as large as 4 V was obtained by program voltage/time (V_{PGM}/t_{PGM}) was 10 V/1 s and erase voltage/time (V_{ERS}/t_{ERS}) was -10 V/1 s, respectively. Furthermore, low voltage and short pulse operation, such as ±6V/2 ms were achieved.

1. Introduction

Recently, the conventional floating gate (FG) type NVM is facing the scaling limits in the terms of coupling ratio, disturbing between the cells and so on [1]. Overcome these issues, charge trapping (CT) type NVM such as MONOS has been attracted much attention [2]. Furthermore, it is necessary to reduce the operation voltage, even for the MONOS NVM with high-k gate insulator. We have reported that excellent electrical characteristics of in-situ formed Hf-based MONOS diodes by electron cyclotron resonance (ECR) plasm sputtering [3].

In this paper, the electrical characteristics of in-situ formed Hf-based MONOS NVM were investigated.

2. Experiment Procedure

Figure 1 shows the experimental procedure used in this research. The in-situ formed Hf-based MONOS NVM was fabricated on p-Si(100) substrate using typical gate-last process [4]. A SiN/SiO_2/p-Si(100) substrate was cleaned by SPM (H_2SO_4:H_2O_2=4:1) and DHF (HF:H_2O=1:100). After the channel stop ion implantation and LOCOS isolation, source and drain (S/D) ion implantation was carried out. Then, the $HfN_{0.5}$(M)/HfO_2(O)/$HfN_{1.0}$(N)/HfO_2(O) structure with thickness of 10/10/3/2 nm, respectively, was in-situ deposited by ECR plasma sputtering at room temperature (RT). Then, post-deposition annealing (PDA) was carried out at 600°C/1 min in N_2 at 1 SLM. After the contact hole formation by RIE in Ar/Cl_2 at 50/20 sccm, the pad and back Al electrodes were formed. Finally, post-metallization annealing (PMA) was carried out at 300°C/10 min in N_2/4.9%H_2 at 1 SLM. The gate length (L) and width (W) of fabricated device was L/W = 2 - 10/90 μm. Figure 2 shows plane-view and schematic cross-section of in-situ formed Hf-based MONOS NVM. Schematic band diagram of Hf-based MONOS structure is illustrated in Fig. 3.

The electrical characteristics of MONOS diodes and in-situ formed Hf-based MONOS NVM were evaluated by C-V, J-V, and I_D-V_G measurements. The operation conditions were set as V_{PGM}/t_{PGM} of 6 V - 10 V/2 ms - 1 s, V_{ERS}/t_{ERS} of -10 V - -6 V/2 ms - 1 s and V_{DS} of 1.5 V.

3. Results and Discussion

Figure 4 (a) shows the C-V characteristics of MONOS diodes. V_{PGM}/t_{PGM} and V_{ERS}/t_{ERS} were set as 10 V/1 s and -10 V/1 s, respectively. A MW of 4.5 V was obtained from the flat-band voltage (V_{FB}) shift between program and erase states. The low leakage current of 1.1 x 10^{-5} A/cm^2 at -10 V was obtained as shown in Fig 4 (b).

Figure 5 shows the I_D-V_G characteristics of in-situ formed Hf-based MONOS NVM. V_{PGM}/t_{PGM}, V_{ERS}/t_{ERS} and V_{DS} were set as 10 V/1 s, -10 V/1 s and 1.5 V, respectively. A MW of 4.1 V was obtained from V_{TH} shift. The hysteresis widths were small as less than 50 mV.

Figure 6 shows the L dependence on V_{TH}. The L was from 2 to 10 μm. Operation condition was same as Fig. 5. It was found that V_{TH} did not depend on L down to 2 μm.

Figure 7 shows the program/erase (P/E) condition dependence on V_{TH}. The operation voltage affected to MW, and MW of 1 V was obtained even for low P/E voltage, such as 6 V /-6 V. In our previous results, the pulse width of 1 s was necessary in the case of MONOS diodes [5, 6]. In-situ formed Hf-based MONOS NVM realized shorter pulse operation, such as 2 ms.

4. Conclusions

We investigated the electrical characteristics of in-situ formed Hf-based MONOS NVM for the first time. In the case of in-situ formed Hf-based MONOS NVM, A MW of 4.1 V was obtained. Furthermore, the low voltage and short pulse operation, such as ±6V/2 ms w.

Acknowledgements

The authors would like to thank Prof. H. Munekata, Prof. Y. Kitamoto, Assistant Prof. N. Nishizawa, Mr. N. Hatakeyama and Mr. M. Suzuki of Tokyo Institute of Technology for their support for this research. The authers also thank the late Prof. Emeritus T. Ohmi, Prof. T. Goto, Prof. R. Kuroda and Assistant Prof. T. Suwa of Tohoku University, Dr. M. Shimada, Mr. M. Hirohara and Mr. I. Tamai of JSW-AFTY for their support and useful discussions for this research. This work was supported by JSPS KAKENHI(JP17J10752).

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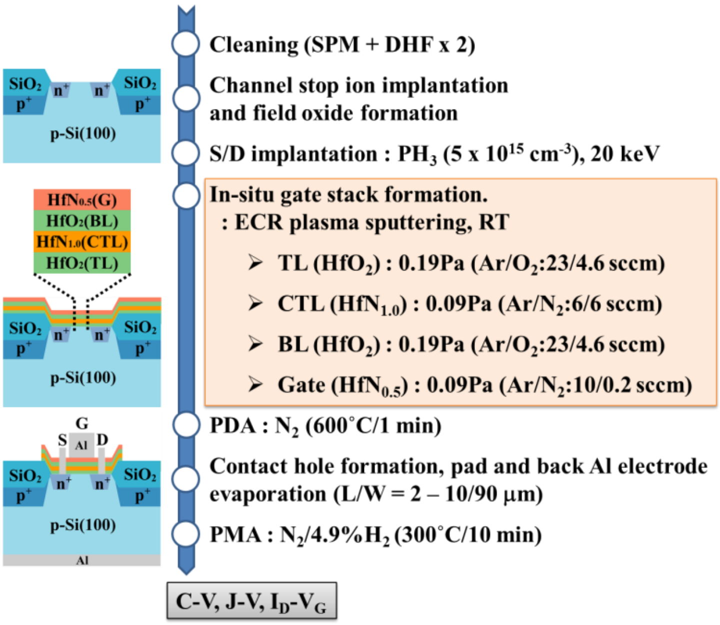


Fig. 1. Experimental procedure.

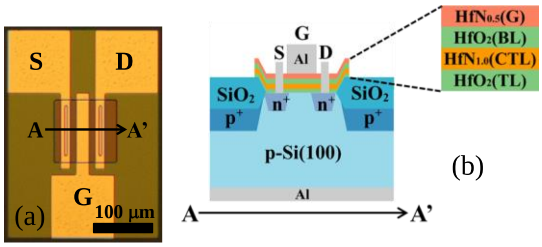


Fig. 2. (a) Plane-view and (b) Schematic cross-section (A-A') of in-situ formed Hf-based MONOS NVM.

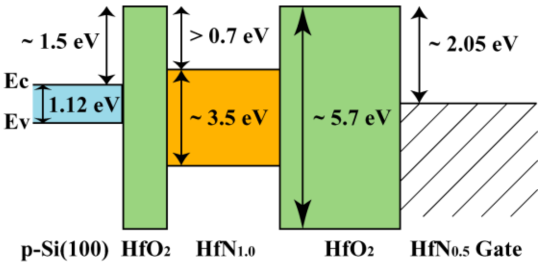
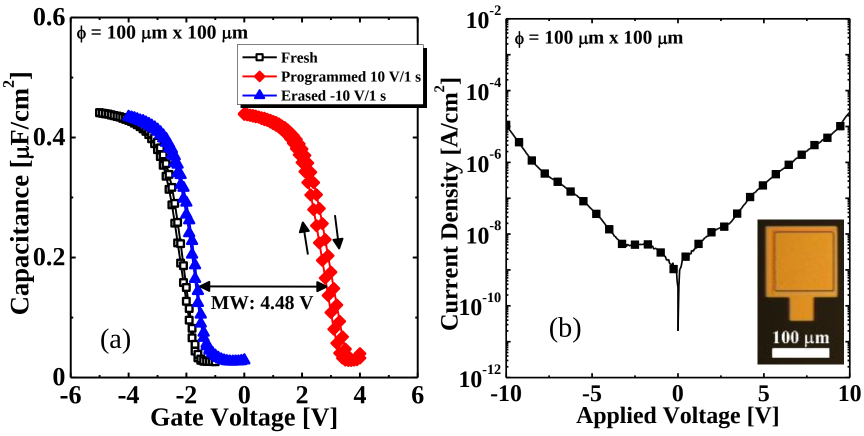


Fig. 3. Schematic energy band diagram of Hf-based MONOS structure.



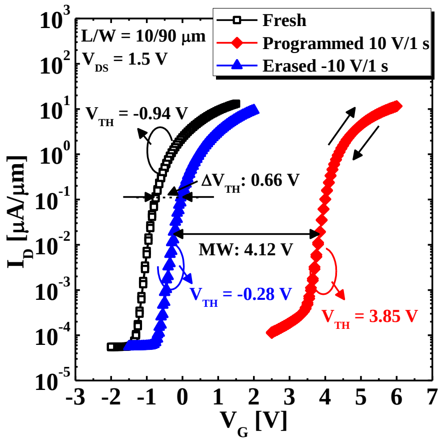


Fig. 4. (a) C-V characteristics of MONOS diodes. V_{PGM}/t_{PGM} was 10 V/1 s and V_{ERS}/t_{ERS} was -10 V/1 s. and (b) J-V characteristics. The inset in Fig. 4 (b) shows a top view of TEG

Fig. 5. I_D-V_G of in-situ formed Hf-based MONOS NVM. V_{PGM}/t_{PGM} was 10 V/1 s and V_{ERS}/t_{ERS} was -10 V/1 s.

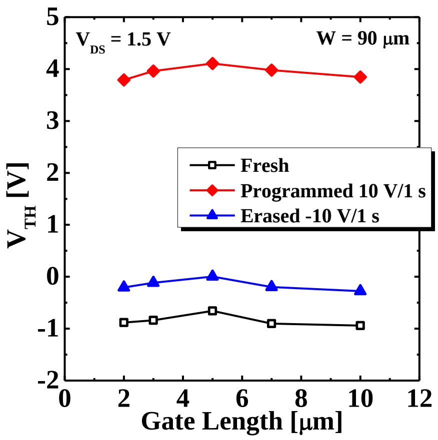


Fig. 6. Gate length dependence on V_{TH}. (L/W = 2-10/90 μm)

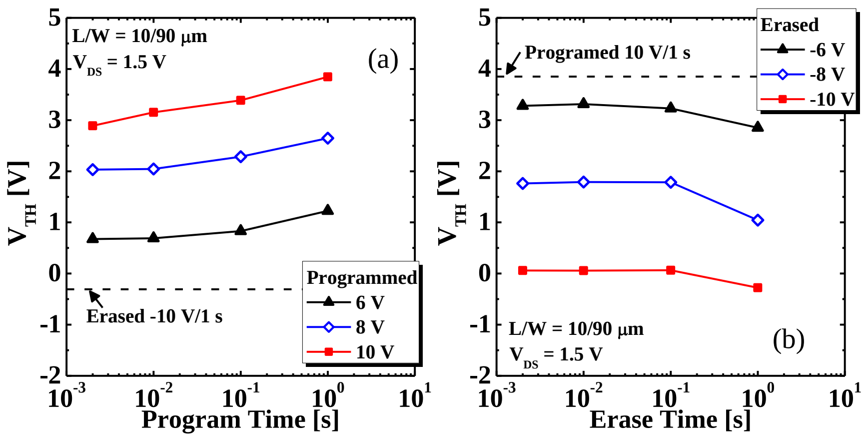


Fig. 7. Pulse width and voltage dependence on V_{TH}. Black dash lines denote V_{TH} before program or erase operation. (a) Program characteristics and (b) erase characteristics.